STIC FAST AND FOCUSED SEARCH
08/02/2007 TLM

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Set     Items    Postings   Description
S1     384929     1704977    S REGISTER?
S2     203297     1481465    S LATCH? OR LATCH()VALVE? OR FLIPFLOP? OR FLIP()FLOP? ?
S3      20936      245541    S S1 AND S2
S4       2259        9829    S PRIMARY OR MAIN OR 1ST OR MASTER OR PRINCIPAL
S5       5645       35032    S SELECT? OR CHOOS? OR CHOIC? OR CHOSE?
S6       2006        6483    S ASSIGN? OR PICK? OR DESIGNAT? OR ELECT???
S7          7          14    S OPT OR OPTS OR OPTING OR OPTED
S8       5822       45306    S PLURAL? OR MULTI OR MULTIPLE OR MULTIPLICIT? OR MULTITUD? OR
SEVERAL? OR NUMEROUS? OR MANY OR ARRAY
S9       7820       58746    S SECOND? OR 2ND OR ALTERNAT? OR BACKUP? OR SLAVE OR REDUNDAN?
S10      8355       41846    S SINGLE OR ONE OR UNIQUE? OR SPECIFIC OR PARTICULAR OR SOLE
S11      2011       11891    S CLOCK()CYCLE? OR CYCLE? OR CLOCKCYCL? OR CLOCK()INTERVAL?
S12      4339       19187    S SWAP? OR TRADE? OR TRADING? OR SWITCH??? OR INTERCHANG? OR
SUBSTITUT?
S13       457        1501    S EXCHANG? OR SUPPLANT? OR SUPERCED? OR SUPERCESS?
S14        17         548    S MULTITHREAD? OR (MULTI OR MULTIPLE OR MULTIPLICIT? OR
MULTITUD? OR SEVERAL? OR NUMEROUS? OR MANY OR ARRAY)(2W)THREAD?
S15      8442       20389    S IC=G06F?
S16      5457        8517    S MC=T01?
S17        17         954    S S3 AND S14
S18        17        1048    S S17 AND S15:S16
S19        17        1042    IDPAT (sorted in duplicate/non-duplicate order)
S20        17        1042    IDPAT (primary/non-duplicate records only)
S21     20919      245133    S S3 NOT S18
S22      3864       92488    S S21 AND (S5:S7 OR S12:S13)(10N)S2
S23       197        9882    S S22 AND (S4 OR S8?S9)(10N)S2
S24        88        4203    S S22 AND S10(5N)S11
S25         6         760    S S23 AND S24
S26         6         760    IDPAT (sorted in duplicate/non-duplicate order)
S27         6         760    IDPAT (primary/non-duplicate records only)
S28       273       12956    S S23:S24 NOT S25
S29      1357       71604    S S22 AND (S4 OR S8:S9)(10N)S2
S30        50        4720    S S29 AND S24
S31        44        3853    S S30 NOT S25
S32        44        3542    IDPAT (sorted in duplicate/non-duplicate order)
S33        44        3542    IDPAT (primary/non-duplicate records only)
S34      1395       78372    S S28:S29
S35      1345       73868    S S34 NOT S30
S36        17        1697    S S35 AND S12:S13 AND S11 AND S8 AND S5:S7
S37        17        1648    IDPAT (sorted in duplicate/non-duplicate order)
S38        17        1648    IDPAT (primary/non-duplicate records only)
 ; show files
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[File 347] **JAPIO** Dec 1976-2007/Dec(Updated 070702)

[File 350] **Derwent WPIX** 1963-2007/UD=200748

**File 350: DWPI has been enhanced to extend content and functionality of the database. For more info, visit http://www.dialog.com/dwpi/.*

FOR. PATENT LIT/ BIBLIOG. FILES

?

20/5,K/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0013059487 *Drawing available*
WPI Acc no: 2003-139229/200313
XRPX Acc No: N2003-110553
Multi-threading processor used in computer, has thread control unit which provides thread control signal to hold latches and registers for selecting specified thread
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: EICKEMEYER R J; HOFSTEE H P; MOORE C R; NAIR R

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20020156999	A1	20021024	US 2001838461	A	20010419	200313	B

Priority Applications (no., kind, date): US 2001838461 A 20010419

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20020156999	A1	EN	11	5	

Alerting Abstract US A1
NOVELTY - The **registers** and hold **latches** in the **multi- threading register** file, store the data representing two instruction threads. A thread control unit (216) provides a thread control signal to the hold **latches** and the **registers** for selecting a thread.
DESCRIPTION - An INDEPENDENT CLAIM is included for data processing system.
USE - For symmetric multiprocessor (SMP) system used in computer.
ADVANTAGE - The cost of implementing the **multi-threading** processor is reduced. The use of processor's resource is maintained by switching between two types of **multi-threading**, thus when long latency occurs in one thread, the execution of the other thread is not slowed down.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the reduced instruction set chip (RISC) processor.
216 Thread control unit

Title Terms /Index Terms/Additional Words: MULTI; THREAD; PROCESSOR; COMPUTER; CONTROL; UNIT; SIGNAL; HOLD; **LATCH**; **REGISTER**; SELECT; SPECIFIED

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/00			Main		"Version 7"

US Classification, Issued: 712228000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): **T01-F02C**; **T01-F03B**; **T01-M02C**

Multi-threading processor used in computer, has thread control unit which provides thread control signal to hold latches and registers for selecting specified thread Original Titles: Mixed-mode hardware **multithreading Alerting Abstract** ...NOVELTY - The **registers** and hold **latches** in the **multi-threading register** file, store the data representing two instruction threads. A thread control unit (216) provides a thread control signal to the hold **latches** and the **registers** for selecting a thread. ...ADVANTAGE - The cost of implementing the **multi-threading** processor is reduced. The use of processor's resource is maintained by switching between two types of **multi-threading**, thus when long latency occurs in one thread, the execution of the other thread is not slowed down... **Title Terms** .../Index Terms/Additional Words: **LATCH**; **REGISTER**; **Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-009/00** Main Manual Codes (EPI/S-X): **T01-F02C**... ...**T01-F03B**... ...**T01-M02C** Original Publication Data by Authority**Original Abstracts:** A mixed-mode **multithreading** processor is provided. **In** one embodiment, the multi-mode **multithreading** processor includes a **multithreaded register** file with **a plurality** of **registers**, a thread control **unit**, and a plurality of hold **latches**. Each of the **hold latches** and **registers** stores **data** representing **a** first instruction thread and a second instruction thread. The thread control unit provides thread control signals to each of the hold **latches** and **registers** selecting **a** thread **using** the data. The thread control unit provides control signals for interleaving **multithreading** except when a **long** latency operation is detected in one of the threads. During a predetermined period corresponding approximately to the duration of the long latency operation, the thread control unit places the processor in a mode in which only instructions corresponding to the other thread are read out of the hold **latches** and **registers**. Once **the** predetermined **period** of time has expired, the processor returns to interleaving **multithreading. Claims:** What is claimed is: **1**. A **multithreading** processor, comprising: a thread control unit; a **multithreaded register** file having a plurality of **registers**; and a plurality of hold **latches, wherein** each of a plurality of **the registers** in the **multithreaded register** file and **each** of a plurality of the hold **latches** stores data **representing** a first **instruction thread** and a second instruction thread; and the thread control **unit** provides a thread control signal to said hold **latches** and **registers** selecting a thread using said data.

20/5,K/4 (Item 4 from file: 350) **Links**
Derwent WPIX

0012458561 *Drawing available*
WPI Acc no: 2002-404495/200243
Related WPI Acc No: 2006-788243
XRPX Acc No: N2002-317520
Data synchronization processing element for data processing applications includes pipeline register with multiple-bit selection switch
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: CHAMDANI J I; RAMAN R; SINGH G P

Patent Family (3 patents, 94 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2002015398	A2	20020221	WO 2001US25553	A	20010814	200243	B
AU 200183383	A	20020225	AU 200183383	A	20010814	200245	E
US 6420903	B1	20020716	US 2000638338	A	20000814	200248	E

Priority Applications (no., kind, date): US 2000638338 A 20000814

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2002015398	A2	EN	34	11		
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW					
AU 200183383	A	EN			Based on OPI patent	WO 2002015398

Alerting Abstract WO A2
NOVELTY - Data in a data path is synchronized by a pipeline **register** that has a driver and a number of switched storage elements (110) coupled to the driver. The driver drives storage elements selected by a multiple-bit selection switch.
DESCRIPTION - An INDEPENDENT CLAIM is included for:

1. a method of operating a pipeline **register**
2. an integrated circuit device for synchronization of data in a data path

USE - For data processing applications.

ADVANTAGE - The system reduces the amount of additional resources for storing inactive states and switching between states.
DESCRIPTION OF DRAWINGS - The drawing shows a schematic block diagram of a pipeline for a processor that utilizes multiple-bit **register flip-flop**.
110 storage element

Title Terms /Index Terms/Additional Words: DATA; SYNCHRONISATION; PROCESS; ELEMENT; APPLY; PIPE; **REGISTER**; MULTIPLE; BIT; SELECT; SWITCH

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-0009/38	A	I		R	20060101
G06F-0009/38	C	I		R	20060101

US Classification, Issued: 326095000, 326098000, 326093000

File Segment: EPI;
DWPI Class: U22; W01
Manual Codes (EPI/S-X): U22-A04C; U22-D04A; W01-A04

Data synchronization processing element for data processing applications includes pipeline register with multiple-bit selection switch Original Titles: High speed multiple-bit **flip-flop**. ... ...HIGH SPEED MULTIPLE-BIT **FLIP-FLOP Alerting Abstract** ...NOVELTY - Data in a data path is synchronized by a pipeline **register** that has a driver and a number of switched storage elements (110) coupled to the driver. The driver drives storage elements selected by a multiple... ... a method of operating a pipeline **register** an integrated circuit device for synchronization of data in a data path... ... DESCRIPTION OF DRAWINGS - The drawing shows a schematic block diagram of a pipeline for a processor that utilizes multiple-bit **register flip-flop.Title Terms** .../Index Terms/Additional Words: **REGISTER; Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-0009/38**... **G06F-0009/38**... Original Publication Data by Authority**Original Abstracts:**A vertical **multi-threading** processor includes one or more execution pipelines that are formed from a plurality of multiple-bit pipeline **register flip-flops**. The multiple-bit pipeline **register flip-flops** supply multiple storage bits. The individual bits of a multiple-bit pipeline **register flip-flop** store data for one of respective **multiple threads** or processes. When an executing (first) process stalls due to a stall condition, for example a cache miss, an active bit of the multiple-bit **register flip-flop** is stalled, removed from activity on the pipeline, and a previously inactive bit becomes active for executing a previously inactive (second) process. All states of the stalled first process are preserved in a temporarily inactive bit of the individual multiple-bit **register flip-flop** in each pipeline stage... ... A vertical **multi-threading** processor (100) includes one or more execution pipelines (200) that are formed from a plurality of multiple-bit pipeline **register flip-flops** (400). The multiple-bit pipeline **register flip-flops** supply multiple storage bits. The individual bits of a multiple-bit pipeline **register flip-flop** store data for one of respective **multiple threads** or processes. When an executing (first) process stalls due to a stall condition, for example a cache miss, an active bit of the multiple-bit **register flip-flop** is stalled, removed from activity on the pipeline, and a previously inactive bit becomes active for executing a previously inactive (second) process. All states of the stalled first process are preserved in a temporarily inactive bit of the individual multiple-bit **register flip-flop** in each pipeline stage... **Claims:**A pipeline **register** for synchronizing data in a data path comprising:a driver;a plurality of

switched storage elements coupled to the driver, the driver for driving a...

20/5,K/9 (Item 9 from file: 350) **Links**
Derwent WPIX

0010774786 *Drawing available*
WPI Acc no: 2001-389308/200141
XRPX Acc No: N2001-286326
Multi-thread processor for commercial computer applications, couples non-stalling component with multi-thread execution pathways, so that pathways are converged into single-pathway including non-stalling component
Patent Assignee: CHAMDANI J I (CHAM-I); JOY W N (JOYW-I); LAUTERBACH G (LAUT-I); SUN MICROSYSTEMS INC (SUNM); TREMBLAY M (TREM-I)
Inventor: CHAMDANI J I; JOY W N; LAUTERBACH G; TREMBLAY M; JOY W

Patent Family (6 patents, 23 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2000068778	A2	20001116	WO 2000US12800	A	20000509	200141	B
US 20020138717	A1	20020926	US 1999309734	A	19990511	200265	E
			US 2002154076	A	20020523		
US 6542991	B1	20030401	US 1999309734	A	19990511	200324	E
US 20030191927	A1	20031009	US 1999309734	A	19990511	200367	E
			US 2003403406	A	20030331		
US 6801997	B2	20041005	US 1999309734	A	19990511	200465	E
			US 2002154076	A	20020523		
US 7185185	B2	20070227	US 1999309734	A	19990511	200718	E
			US 2003403406	A	20030331		

Priority Applications (no., kind, date): US 1999309734 A 19990511; US 2002154076 A 20020523; US 2003403406 A 20030331

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2000068778	A2	EN	71	18		
National Designated States,Original	IL JP KR SG					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 20020138717	A1	EN			Division of application	US 1999309734
US 20030191927	A1	EN			Continuation of application	US 1999309734
					Continuation of patent	US 6542991
US 6801997	B2	EN			Division of application	US 1999309734
US 7185185	B2	EN			Continuation of application	US 1999309734
					Continuation of patent	US 6542991

Alerting Abstract WO A2

NOVELTY - The processor uses a **multi-thread** execution pipeline with execution pathways allocated to respective execution threads. A non-stalling component is coupled to **multi-thread** execution pathways, so that the pathways are converged into single-pathway including the non-stalling component.

DESCRIPTION - The non-stalling component is selected from caches, translation look-aside buffers (TLBs), load buffer asynchronous interfaces and external memory management unit (MMU) interface. A thread tagging logic coupled to the non-stalling component, sets a thread identifier (TID) tag identifying threads in non-stalling component. The non-stalling component shared between **several threads**, maintains compatibility among threads by physical duplication of structures and by verifying the communication status after transfer of thread. An INDEPENDENT CLAIM is also included for operating method of **multi-thread** processor.

USE - **Multi-thread** processor for commercial computer applications including embedded, desktop and server applications, and for handling operations such as OLTP, DSS, data mining, financial forecasting, mechanical and electronic computer-aided design (MCAD/ECAD). And also for web servers, data servers, etc.

ADVANTAGE - Reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical and horizontal **multi-threadings**. Increases system parallelism by forming several processor cores in a single die. Advances in on-chip multiprocessor horizontal threading, are realized, as the processor core sizes are reduced by technological advancements. Vertical **multi-threading** overcomes or hides cache miss stalls, thereby improves performance in commercial multiprocessor and **multi-threading** applications.

DESCRIPTION OF DRAWINGS - The figure shows the schematic perspective diagram of multi-dimensional **register** file.

Title Terms /Index Terms/Additional Words: MULTI; THREAD; PROCESSOR; COMMERCIAL; COMPUTER; APPLY; COUPLE; NON; STALL; COMPONENT; EXECUTE; PATH; SO; CONVERGE ; SINGLE

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-0012/08	A	I		R	20060101
G06F-0009/38	A	I		R	20060101
G06F-0012/12	A	I	F	B	20060101
G06F-0012/08	C	I		R	20060101
G06F-0009/38	C	I		R	20060101
G06F-0012/12	C	I		B	20060101

US Classification, Issued: 712023000, 712235000, 712228000, 709108000, 712228000, 712229000, 712228000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): **T01-C07C2**; **T01-F02C**; **T01-F03B1**; **T01-H08**

Multi-thread processor for commercial computer applications, couples non-stalling component with

multi-thread execution pathways, so that pathways are converged into single-pathway including non-stalling component Original Titles:Multiple-thread processor with single-thread interface shared among threads... ...**Multiple-thread** processor with in-pipeline, thread selectable storage... ...**Multiple-thread** processor with single-thread interface shared among threads... ...**Multiple-thread** processor with single-thread interface shared among threads... ...**Multiple-thread** processor with in-pipeline, thread selectable storage... ...**MULTIPLE-THREAD** PROCESSOR WITH SINGLE-THREAD INTERFACE SHARED AMONG THREADS **Alerting Abstract** ...NOVELTY - The processor uses a **multi-thread** execution pipeline with execution pathways allocated to respective execution threads. A non-stalling component is coupled to **multi-thread** execution pathways, so that the pathways are converged into single-pathway including the non-stalling component. ...logic coupled to the non-stalling component, sets a thread identifier (TID) tag identifying threads in non-stalling component. The non-stalling component shared between **several threads**, maintains compatibility among threads by physical duplication of structures and by verifying the communication status after transfer of thread. An INDEPENDENT CLAIM is also included for operating method of **multi-thread** processor... ...USE - **Multi-thread** processor for commercial computer applications including embedded, desktop and server applications, and for handling operations such as OLTP, DSS, data mining, financial forecasting, mechanical and... ...ADVANTAGE - Reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical and horizontal **multi-threadings**. Increases system parallelism by forming several processor cores in a single die. Advances in on-chip multiprocessor horizontal threading, are realized, as the processor core sizes are reduced by technological advancements. Vertical **multi-threading** overcomes or hides cache miss stalls, thereby improves performance in commercial multiprocessor and **multi-threading** applications... ...DESCRIPTION OF DRAWINGS - The figure shows the schematic perspective diagram of multi-dimensional **register** file. **Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-0012/08**... ...**G06F-0009/38**... ...**G06F-0012/12 G06F-0012/08**... ...**G06F-0009/38**... ...**G06F-0012/12** Manual Codes (EPI/S-X): **T01-C07C2**... ...**T01-F02C**... ...**T01-F03B1**... ...**T01-H08** Original Publication Data by Authority...**Original Abstracts:**A processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical **multithreading** and horizontal **multithreading**. Vertical **multithreading** permits overlapping or "hiding" of cache miss wait times. In vertical **multithreading, multiple** hardware **threads** share the same processor pipeline. A hardware thread is typically a process, a lightweight process, a native thread, or the like in an operating system that supports **multithreading**. Horizontal **multithreading** increases parallelism within the processor circuit structure, for example within a single integrated circuit die that makes up a single-chip processor. To further increase... ... A processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical **multithreading** and horizontal **multithreading**. Vertical **multithreading** permits overlapping or "hiding" of cache miss wait times. In vertical **multithreading, multiple** hardware **threads** share the same processor pipeline. A hardware thread is typically a process, a lightweight process, a native thread, or the like in an operating system that supports **multithreading**. Horizontal **multithreading** increases parallelism within the processor circuit structure, for example within a single integrated circuit die that makes up a single-chip processor. To further increase... **Claims:**What is claimed is:**1**. A processor comprising:a **multiple-thread** execution pipeline including a plurality of functional units allocated to an execution thread of a plurality of execution threads; anda single-thread interface coupled... ... What is claimed is:**1**. A vertically **multi-threaded** processor comprising:a **register** file structure replicated to simultaneously represent **register** state for at least two threads; andat least one pipeline sharable amongst the two threads and coupled to the **register** file structure, the sharable pipeline including replicated thread selectable storage elements defined therein, whereby the processor freezes in the pipeline, for later resumption, active state... .:. What is claimed is:1. A processor comprising:a **multiple-thread** execution pipeline including a plurality of functional units allocated to an execution thread of a plurality of execution threads; anda single-thread interface coupled... ... thread interface being shared among threads and maintaining thread compatibility by physical duplication of structures and by verifying

communication status after thread transfer, wherein:the **multiple-thread** execution pipeline includes a plurality of pulse-based high-speed multiple-bits **flip-flops**, the pulse-based high-speed multiple-bits **flip-flops** having a **latch** structure coupled to a plurality of select-bus lines, the select-bus lines selecting data in the pulsed-based high-speed multiple-bits **flip-flops** corresponding to an active thread from among the plurality of execution threads... ... What is claimed is:1. A processor comprising:a **multiple-thread** execution pipeline including a plurality of pipelines respectively allocated to a plurality of execution threads, respective ones of the plurality of pipelines to execute the... ... of the plurality of pipelines is to execute more than one of the plurality of execution threads in a second thread dimension, and wherein the **multiple-thread** execution pipeline includes storage elements for holding the plurality of threads;a plurality of shared components coupled to the **multiple-thread** execution pipeline, the shared components being coupled in a sequence so that the plurality of pipelines converge into the sequence of shared components, the shared components being logic components that control but do not hold threads;a cache control unit coupled to the **multiple-thread** execution pipeline;an L1 cache coupled to the cache control unit; andanti-aliasing logic coupled to the L1 cache so that the L1 cache... ... What is claimed is:1. A vertically **multi-threaded** processor comprising: a **register** file structure replicated to simultaneously represent **register** state for at least two threads; andat least one pipeline sharable amongst the two threads and coupled to the **register** file structure, the sharable pipeline including replicated thread selectable storage elements defined therein, whereby the processor freezes in the pipeline, for later resumption, active state...

20/5,K/11 (Item 11 from file: 350) **Links**
Derwent WPIX

0010555362 *Drawing available*
WPI Acc no: 2001-158945/200116
XRPX Acc No: N2001-115846
Multiple thread processor has execution pipe line coupled to machine state logic of processing unit and shared among multiple execution threads by vertical threading operation
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: CHAMDANI I; CHAMDANI J I; JOY N; JOY W N; LAUTERBACH G; TREMBLAY M

Patent Family (6 patents, 24 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2000068779	A2	20001116	WO 2000US12931	A	20000510	200116	B
EP 1179195	A2	20020213	EP 2000930612	A	20000510	200219	E
			WO 2000US12931	A	20000510		
EP 1179195	B1	20040818	EP 2000930612	A	20000510	200455	E
			WO 2000US12931	A	20000510		
DE 60013115	E	20040923	DE 60013115	A	20000510	200462	E
			EP 2000930612	A	20000510		
			WO 2000US12931	A	20000510		
US 6938147	B1	20050830	US 1999309732	A	19990511	200557	E
DE 60013115	T2	20050901	DE 60013115	A	20000510	200559	E
			EP 2000930612	A	20000510		
			WO 2000US12931	A	20000510		

Priority Applications (no., kind, date): US 1999309732 A 19990511

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2000068779	A2	EN	70	18		
National Designated States,Original	IL JP KR RU SG					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1179195	A2	EN			PCT Application	WO 2000US12931
					Based on OPI patent	WO 2000068779
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
EP 1179195	B1	EN			PCT Application	WO 2000US12931
					Based on OPI patent	WO 2000068779

Regional Designated States,Original	DE FR GB IE					
DE 60013115	E	DE			Application	EP 2000930612
					PCT Application	WO 2000US12931
					Based on OPI patent	EP 1179195
					Based on OPI patent	WO 2000068779
DE 60013115	T2	DE			Application	EP 2000930612
					PCT Application	WO 2000US12931
					Based on OPI patent	EP 1179195
					Based on OPI patent	WO 2000068779

Alerting Abstract WO A2
NOVELTY - IC is equipped with processing unit having machine state logic (310,312) including multiple shadow machine states respectively allocated to **multiple** execution **threads**. Execution pipeline (314) is coupled to machine state logic and is shared among execution threads by vertical threading. Load/store units (316,318) are coupled to the execution pipe line and are shared among the execution threads.
USE - For database handling operations such as OLTP, DSS, data mining, financial forecasting, mechanical and electronic computer aided design, webservers and data servers.
ADVANTAGE - Provides improved **multithreading** circuits and operating methods that are economical in resources and avoid costly overhead which reduces processor performance. Allows processor to enter and exit the exception handler immediately without waiting to drain the pipeline or queues and without the inherent timing penalty of the operating system's software saving and restoring of **registers**.
DESCRIPTION OF DRAWINGS - The figure shows the schematic block diagram depicting a design configuration for a single vertically threaded processor.
310,312 Machine state logic
314 Execution pipe line
316,318 Load/store units

Title Terms /Index Terms/Additional Words: MULTIPLE; THREAD; PROCESSOR; EXECUTE; PIPE; LINE; COUPLE; MACHINE; STATE; LOGIC; PROCESS; UNIT; SHARE; VERTICAL; OPERATE

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/00			Main		"Version 7"

US Classification, Issued: 712028000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): **T01-J05A1**; **T01-J05B4M**

Multiple thread processor has execution pipe line coupled to machine state logic of processing unit and shared among multiple execution threads by vertical threading operation ...Original Titles:PROCESSOR WITH

MULTIPLE-THREAD, VERTICALLY-**THREADED** PIPELINE... ...PROCESSOR WITH **MULTIPLE-THREAD**, VERTICALLY-**THREADED** PIPELINE AND OPERATING METHOD THEREOF... ...PROCESSEUR DOTE D'UN PIPELINE **MULTITHREAD**, A THREADS VERTICAUX ET SA METHODE OPERATOIRE... ...Processor with **multiple-thread**, vertically-**threaded** pipeline... ...PROCESSOR WITH **MULTIPLE-THREAD**, VERTICALLY-**THREADED** PIPELINE... **Alerting Abstract** ...NOVELTY - IC is equipped with processing unit having machine state logic (310,312) including multiple shadow machine states respectively allocated to **multiple** execution **threads**. Execution pipeline (314) is coupled to machine state logic and is shared among execution threads by vertical threading. Load/store units (316,318) are coupled... ...ADVANTAGE - Provides improved **multithreading** circuits and operating methods that are economical in resources and avoid costly overhead which reduces processor performance. Allows processor to enter and exit the exception... ...immediately without waiting to drain the pipeline or queues and without the inherent timing penalty of the operating system's software saving and restoring of **registers**. **Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-009/00** Main Manual Codes (EPI/S-X): **T01-J05A1**... ...**T01-J05B4M** Original Publication Data by Authority**Original Abstracts:**A processor (300) reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical **multithreading** and horizontal **multithreading**. **Vertical multithreading** permits **overlapping** or "**hiding**" of cache miss wait times. In vertical **multithreading, multiple** hardware **threads share the** same **processor** pipeline (314). A hardware thread is typically a process, a lightweight process, a native thread, or the like in an operating system that supports **multithreading**. Horizontal **multithreading** increases **parallelism** within **the** processor circuit structure, for example within a single integrated circuit die that makes up a single-chip processor. To further increase system parallelism in some... ... A processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical **multithreading** and horizontal **multithreading**. Vertical **multithreading** permits overlapping or "**hiding**" of cache **miss** wait **times**. In vertical **multithreading, multiple** hardware **threads** share the same processor pipeline. **A hardware thread is** typically a process, a lightweight process, a native thread, or the like in an operating system that supports **multithreading**. Horizontal **multithreading** increases parallelism within the processor circuit **structure**, for **example** within a single integrated circuit die that makes up a single-chip processor. To further increase system parallelism in some processor embodiments, multiple processor cores... ... A processor (300) reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical **multithreading** and horizontal **multithreading**. Vertical **multithreading** permits overlapping or "hiding" of cache miss wait **times**. In vertical **multithreading, multiple hardware threads** share the same processor pipeline (314). A hardware thread is **typically a** process, **a** lightweight process, a native thread, or the like in an operating system that supports **multithreading**. Horizontal **multithreading** increases parallelism within the processor circuit structure, for example within a **single** integrated **circuit** die that makes up a single-chip processor. To further increase system parallelism in some processor embodiments, multiple processor cores are formed in a single die.Advances in on-chip multiprocessor **horizontal threading** are gained as processor core sizes are reduced through technological advancements... ...**Claims:**Prozessor-Pipeline (314), die in der Lage ist, gleichzeitig eine Vielzahl von Ausfuhrungsthreads einschliesslich einem oder mehrerer Schattenthreads unter Verwendung von Pipelineregistern aus Multi-Bit **Flip-Flops** (400) zu **halten, wobei** immer nur einer aus der Vielzahl der Ausfuhrungsthreads gleichzeitig aktiv ausgefuhrt wird; undeine Threadsteuerlogik (310, 312), die mit der gemeinsamen Prozessor-Pipeline verbunden ist... ... comprising:a shared processor pipeline (314) that is capable of concurrently holding a plurality of execution threads including one or more shadow threads using pipeline **registers** of **multi**-bit **flip-flops** (400), one of the plurality of execution threads **being** actively executed at **one time**; anda thread control logic (310, 312) coupled to the shared processor pipeline that is capable of controlling the shared processor pipeline to select a... ... de la possession simultanee d'une pluralite de threads d'execution, incluant un ou plusieurs threads ombre, utilisant des registres de canaux de donnees de **flip-flops** multi-bits (400), l'une de la pluralite de threads d'execution etant executee activement une fois: etune logique de commande **pour les threads**

(310, 312) couplee au canal de donnees du processeur partage qui est capable de commander au canal de donnees du processeur partage de selectionner un... ... 1. A processor comprising:a shared processor pipeline that includes therein a plurality of multiple-bit **flip-flops**, each multiple-bit **flip-flop** capable of concurrently holding in the shared processor pipeline, at least a portion of thread state for a plurality of execution treads, one of the **execution threads being actively** executed in the **shared processor** pipeline at a given time; andthread control logic coupled to the shared processor pipeline and cap able of controlling the shared processor pipeline to select thread state for an active one of the execution threads, including the portion of the thread state represented in the multiple-bit **flip-flops** of the shared processor pipeline.

20/5,K/12 (Item 12 from file: 350) **Links**
Derwent WPIX

0010555361 *Drawing available*
WPI Acc no: 2001-158944/200116
XRPX Acc No: N2001-115845
Multi-thread processor for commercial computer applications, has multi-threaded processor core converted from single thread processor core, which maintains terminal connections of single thread processor core
Patent Assignee: CHAMDANI J I (CHAM-I); JOY W N (JOYW-I); LAUTERBACH G (LAUT-I); SUN MICROSYSTEMS INC (SUNM); TREMBLAY M (TREM-I)
Inventor: CHAMDANI J I; JOY W N; LAUTERBACH G; TREMBLAY M

Patent Family (2 patents, 23 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2000068777	A2	20001116	WO 2000US12797	A	20000509	200116	B
US 20030014612	A1	20030116	US 1999309730	A	19990511	200308	E

Priority Applications (no., kind, date): US 1999309730 A 19990511

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
WO 2000068777	A2	EN	70	18	
National Designated States,Original	IL JP KR SG				
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE				

Alerting Abstract WO A2
NOVELTY - The processor includes a **multi-threaded** processor core which is converted from a single-thread processor core, using **multi**-bit, **thread** selectable **flip-flops**. The **multithreaded** processor core having an aspect ratio, maintains terminal connections of single-thread processor core.
DESCRIPTION - The **multi-threaded** pipeline in the **multi -threaded** processor core, includes **several multi**-bit, **thread**-selectable master-slave **flip-flops** which globally replace the single bit master slave **flip-flops** of single thread processor core, but maintains the same footprint as the single bit master slave **flip flops**. An INDEPENDENT CLAIM is also included for retrofitting method of single-thread processor with **multi-thread** processor.
USE - **Multi-thread** processor for commercial computer applications, and for handling operations such as OLTP, TSS, data mining, financial forecasting, mechanical and electronic computer-aided design, (MCAD/ECAD). And also for web servers, data servers, etc.
ADVANTAGE - Reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical and horizontal **multi threadings**. Increases system parallelism by forming several processor cores in single die. Advances in on-chip multiprocessor horizontal threading, are realized, as the processor core sizes are reduced by technology advancements. During designing, vertical and horizontal **multithreadings** are achieved with minimal retrofitting of existing processor core, thereby reducing logic and physical design changes and avoiding global chip re-routing, recomposing, and the expense of

heavy redesigning of integrated circuits. Vertical **multithreading** provides advantageous effects in sequential and parallel processing applications with frequent context switches, reliably.
DESCRIPTION OF DRAWINGS - The figure shows schematic perspective diagram of multi-dimensional **register** file.

Title Terms /Index Terms/Additional Words: MULTI; THREAD; PROCESSOR; COMMERCIAL; COMPUTER; APPLY; CORE; CONVERT; SINGLE; MAINTAIN; TERMINAL; CONNECT

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/00; G06F-009/30			Main		"Version 7"

US Classification, Issued: 712215000, 712235000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): **T01-F02C**; **T01-H03C**; **T01-H05B1**; **T01-M02C2**

Multi-thread processor for commercial computer applications, has multi-threaded processor core converted from single thread processor core, which maintains terminal connections of single thread processor core
Original Titles:MULTI-THREADED PROCESSOR BY MULTIPLE-BIT **FLIP- FLOP** GLOBAL SUBSTITUTION... ...**MULTI-THREADED** PROCESSOR BY MULTIPLE-BIT **FLIP- FLOP** GLOBAL SUBSTITUTION **Alerting Abstract** ...NOVELTY - The processor includes a **multi-threaded** processor core which is converted from a single-thread processor core, using **multi**-bit, **thread** selectable **flip-flops**. The **multithreaded** processor core having an aspect ratio, maintains terminal connections of single-thread processor core.
DESCRIPTION - The **multi-threaded** pipeline in the **multi -threaded** processor core, includes **several multi**-bit, **thread**-selectable master-slave **flip-flops** which globally replace the single bit master slave **flip-flops** of single thread processor core, but maintains the same footprint as the single bit master slave **flip flops**. An INDEPENDENT CLAIM is also included for retrofitting method of single-thread processor with **multi-thread** processor... ...USE - **Multi-thread** processor for commercial computer applications, and for handling operations such as OLTP, TSS, data mining, financial forecasting, mechanical and electronic computer-aided design, (MCAD/ECAD... ...ADVANTAGE - Reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical and horizontal **multi threadings**. Increases system parallelism by forming several processor cores in single die. Advances in on-chip multiprocessor horizontal threading, are realized, as the processor core sizes are reduced by technology advancements. During designing, vertical and horizontal **multithreadings** are achieved with minimal retrofitting of existing processor core, thereby reducing logic and physical design changes and avoiding global chip re-routing, recomposing, and the expense of heavy redesigning of integrated circuits. Vertical **multithreading** provides advantageous effects in sequential and parallel processing applications with frequent context switches, reliably ... ...DESCRIPTION OF DRAWINGS - The figure shows schematic perspective diagram of multi-dimensional **register** file. **Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-009/00**... ...**G06F-009/30** Main Manual Codes (EPI/S-X): **T01-F02C**... ...**T01-H03C**... ...**T01-H05B1**... ...**T01-M02C2** Original Publication Data by Authority**Original Abstracts:**A processor improves throughput efficiency and exploits increased parallelism by

introducing **multithreading** to an existing **and** mature processor core. The **multithreading** is implemented in **two** steps including vertical **multithreading** and horizontal **multithreading**. **The** processor core **is** retrofitted to support multiple machine states. System embodiments that exploit retrofitting of an existing processor core advantageously leverage hundreds of man-years of hardware and software development by extending the lifetime of a proven processor pipeline generation. A processor implements N-bit **flip-flop** global substitution. **To implement** multiple machine states, the processor converts 1-bit **flip-flops** in storage **cells of** the stalling vertical thread to an N-bit global **flip-flop** where N **is the** number of vertical threads... ... A processor improves throughput efficiency and exploits increased parallelism by introducing **multithreading** to an existing and mature processor core (300). **The multithreading** is implemented in two steps including vertical **multithreading and** horizontal **multithreading**. The processor core is retrofitted **to** support multiple **machine** states. System embodiments that exploit retrofitting of an existing processor core advantageously leverage hundreds of man-years of hardware and software development by extending the lifetime of a proven processor pipeline generation. A processor implements N-bit **flip-flop** global substitution. To implement multiple machine states, **the processor** converts 1-bit **flip-flops** in storage cells of the stalling vertical **thread to** an N-bit global **flip-flop** where N is the number of vertical **threads. Claims:** What is claimed is:**1**. A processor comprising:a **multiple-threaded** processor core converted from a single-thread processor core **and maintaining** area, aspect ratio, and terminal connections of the single-thread processor core.

20/5,K/13 (Item 13 from file: 350) **Links**
Derwent WPIX

0010543662 *Drawing available*
WPI Acc no: 2001-146691/200115
XRPX Acc No: N2001-107394
Multiple thread processor has thread switch logic for switching execution threads according to thread switching mode selected from multiple thread switching modes
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: CHAMDANI J I; JOY W N; LAUTERBACH G; TREMBLAY M

Patent Family (5 patents, 23 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2000068780	A2	20001116	WO 2000US12938	A	20000510	200115	B
US 6341347	B1	20020122	US 1999309733	A	19990511	200208	E
EP 1224535	A2	20020724	EP 2000930618	A	20000510	200256	E
			WO 2000US12938	A	20000510		
EP 1224535	B1	20031001	EP 2000930618	A	20000510	200365	E
			WO 2000US12938	A	20000510		
DE 60005701	E	20031106	DE 60005701	A	20000510	200381	E
			EP 2000930618	A	20000510		
			WO 2000US12938	A	20000510		

Priority Applications (no., kind, date): US 1999309733 A 19990511

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2000068780	A2	EN	75	18		
National Designated States,Original	IL JP KR SG					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1224535	A2	EN			PCT Application	WO 2000US12938
					Based on OPI patent	WO 2000068780
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
EP 1224535	B1	EN			PCT Application	WO 2000US12938
					Based on OPI patent	WO 2000068780
Regional Designated States,Original	DE FR GB					
DE 60005701	E	DE			Application	EP 2000930618

					PCT Application	WO 2000US12938
					Based on OPI patent	EP 1224535
					Based on OPI patent	WO 2000068780

Alerting Abstract WO A2

NOVELTY - **Multiple thread** execution pipeline has multiple pipelines allocated to **multiple** execution **threads**. **Thread** switch logic coupled to the **multiple thread** execution pipeline, switches execution threads according to thread switching mode selected from **multiple thread** switching modes. One thread switching mode is an oblivious mode switching threads for every N selected number of cycles.

DESCRIPTION - An INDEPENDENT CLAIM is also included for method of operating processor.

USE - For database handling operations such as OLTP, DSS, data mining, financial forecasting, mechanical and electronic computer aided design, web servers, data servers.

ADVANTAGE - Provides improved **multi-threading** circuits and operating methods that are economical in resources and avoids costly overhead which reduces processor performance. Allows the processor to enter and exit the exception handler immediately without waiting to drain the pipeline or queues and without inherent timing penalty of the operating system's software saving and restoring of **registers**.

DESCRIPTION OF DRAWINGS - The figure shows the schematic block diagram of anti-aliasing logic for usage in various processor implementations including cache.

Title Terms /Index Terms/Additional Words: MULTIPLE; THREAD; PROCESSOR; SWITCH; LOGIC; EXECUTE; ACCORD; MODE; SELECT

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/00; G06F-009/30			Main		"Version 7"
G06F-009/38; G06F-009/48; G06F-009/52			Secondary		"Version 7

US Classification, Issued: 712228000, 712219000, 712023000, 712245000, 712229000, 709107000, 709106000 , 709108000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): **T01-F03B1**; **T01-M02C2**

Multiple thread processor has thread switch logic for switching execution threads according to thread switching mode selected from multiple thread switching modes Original Titles:THREADUMSCHALTUNGSLOGIK IN EINEM **MULTITHREADPROZESSOR** ... ...THREAD SWITCH LOGIC IN A **MULTIPLE-THREAD** PROCESSOR... ...THREADUMSCHALTUNGSLOGIK IN EINEM **MULTITHREADPROZESSOR**... ...THREAD SWITCH LOGIC IN A **MULTIPLE-THREAD** PROCESSOR... ...Thread switch logic in a **multiple-thread** processor... ...THREAD SWITCH LOGIC IN A **MULTIPLE-THREAD** PROCESSOR **Alerting Abstract** ...NOVELTY - **Multiple thread** execution pipeline has

multiple pipelines allocated to **multiple** execution **threads. Thread** switch logic coupled to the **multiple thread** execution pipeline, switches execution threads according to thread switching mode selected from **multiple thread** switching modes. One thread switching mode is an oblivious mode switching threads for every N selected number of cycles. ...ADVANTAGE - Provides improved **multi-threading** circuits and operating methods that are economical in resources and avoids costly overhead which reduces processor performance. Allows the processor to enter and exit the... ...handler immediately without waiting to drain the pipeline or queues and without inherent timing penalty of the operating system's software saving and restoring of **registers. Class Codes** International Patent Classification IPC Class Level Scope Position Status Version Date **G06F-009/00**... ...**G06F-009/30** Main **G06F-009/38**... ...**G06F-009/48**... ...**G06F-009/52** Manual Codes (EPI/S-X): **T01-F03B1**... ...**T01-M02C2** Original Publication Data by Authority...**Original Abstracts:**that performs a fast thread-switching operation in response to an L1 cache miss stall. The fast thread-switching operation implements one or more of **several thread**-switching methods. **A first thread**-switching operation is "oblivious" thread-switching for every N cycle in which the individual **flip-flops** locally determine **a thread**-switch without notification of stalling. The oblivious technique avoids usage of an extra global interconnection between threads for thread selection. A second thread-switching operation... ... as fast as possible, similar to a clock tree distribution. In some systems, a processor derives a thread select signal that is applied to the **flip-flops** by overloading **a scan** enable (SE) signal of a scannable **flip-flop**. ... ... logic that performs a fast thread-switching operation in response to an L1cache miss stall. The fast thread-switching operation implements one or more of **several thread**-switching methods. A first thread-switching operation **is "oblivious" thread**-switching for every N cycle in which the individual **flip-flops** locally determine a thread-switch without notification **of stalling**. The oblivious technique avoids usage of an extra global interconnection between threads for thread selection. A second thread-switching operation is "semi-oblivious" thread-switching... ... as fast as possible, similar to a clock tree distribution. In some systems, a processor derives a thread select signal that is applied to the **flip-flops** by overloading a scan enable (SE) signal of a scannable **flip-flop**. ... ... that performs a fast thread-switching operation in response to an L1 cache miss stall. The fast thread-switching operation implements one or more of **several thread**-switching methods. A first thread-switching operation is "oblivious" thread-switching for every N cycle in which **the individual flip-flops** locally determine a thread-switch without notification of stalling. The oblivious technique avoids usage of an extra **global interconnection** between threads for thread selection. A second thread-switching operation is "semi-oblivious" thread-switching for use with an existing "pipeline stall" signal (if any... ... as fast as possible, similar to a clock tree distribution. In some systems, a processor derives a thread select signal that is applied to the **flip-flops** by overloading a scan enable (SE) signal of a scannable **flip-flop. Claims:**Prozessor, umfassend:eine **Multithread**- Executionpipeline (314) mit **einer** Vielzahl von Pipelines, die jeweils einer Vielzahl von Executionthreads (122, 124, 126 und 128) zugeordnet sind; undeine Threadumschaltlogik (610), die mit der **Multithread**-Executionpipeline gekoppelt ist, wobei die **Threadumschaltlogik** die Executionthreads nach einer Thread-Umschaltbetriebsweise umschaltet, die aus einer Vielzahl von Thread-Umschaltbetriebsweisen ausgewahlt wird, wobei die **Multithreadstruktur** gleichzeitig Daten von mehreren Threads **unter** Verwendung von **Multiple**-Bit-**Flip-Flops** reprasentiert.A processor comprising;a **multiple-thread** execution pipeline (314) including a plurality of pipelines respectively allocated to a **plurality of** execution **threads** (122, 124, 126, and 128); anda thread switch logic (610) coupled to the **multiple-thread** execution pipeline, the thread switch logic switching execution threads according to a thread switching **mode selected** from among a plurality of thread switching modes wherein a **multiple-threaded structure** concurrently represents data for **multiple threads** using **multiple-bit flip-flops**.... ... modes de commutation de processus elementaires dans lesquels une structure a processus elementaires multiples represente simultanement des donnees pour des processus elementaires multiples utilisant des **flip-flop** a bits multiples.A processor comprising:a **multiple-thread** execution pipeline including a plurality of pipelines respectively allocated to a plurality of execution threads; anda thread switch logic coupled to the **multiple-thread** execution pipeline, the thread switch logic that **switches execution threads** according to a thread switching mode selected from among a plurality of thread switching modes.

27/5,K/1 (Item 1 from file: 350) **Links**
Derwent WPIX

THIS APPLICATION

0014966023 *Drawing available*
WPI Acc no: 2005-313820/200532
XRPX Acc No: N2005-256507

Integrated circuit for computer system, has register file bit comprising context switch mechanism causing data on data output of primary latch to be written to secondary latch and vice versa in single clock cycle

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: LUICK D A

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050081018	A1	20050414	US 2003682134	A	20031009	200532	B

Priority Applications (no., kind, date): US 2003682134 A 20031009

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050081018	A1	EN	9	5	

27/5,K/2 (Item 2 from file: 350) **Links**
Derwent WPIX

0008126392 *Drawing available*
WPI Acc no: 1997-225671/199720
XRPX Acc No: N1997-186759
Latched synchronous output circuit for e.g. cache SRAM for pentium - has latch and parallel slave latch with incoming data inverted by swapping inputs from sense amplifier and sensing data on global bar
Patent Assignee: SGS THOMSON MICROELTRN INC (SGSA)
Inventor: MCCLURE D C

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5619456	A	19970408	US 1996588901	A	19960119	199720	B

Priority Applications (no., kind, date): US 1996588901 A 19960119

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5619456	A	EN	33	15	

Alerting Abstract US A
The synchronous output buffer device includes a data input terminal, three clock controlled transfer gates, and two **latch** circuits. The first gate (68) is enabled on **one** phase of a **clock cycle** and disabled on another. The second gate is coupled to the output of the first **latch** (75) and has its output coupled to an input terminal of an output driver circuit (95). The third gate is coupled between the input of the first **latch** and an inverted output of the first **latch**. The third gate is disabled on the first phase of the clock and enabled on the second to maintain the input data received on the first phase of the clock during the second phase of the clock when the first transfer gate is disabled and to accept new input data on the first phase of the clock when the first transfer gate is disabled.
USE/ADVANTAGE - Also for DRAM, EEPROM and flash EEPROM. High speed output buffer due to clocked parallel operation. Slave **latch** holds input data while additional data is presented for input.

Title Terms /Index Terms/Additional Words: **LATCH**; SYNCHRONOUS; OUTPUT; CIRCUIT; CACHE; SRAM; PARALLEL; SLAVE; INCOMING; DATA; INVERT; INPUT; SENSE; AMPLIFY ; GLOBE; BAR

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G11C-013/00			Main		"Version 7"

US Classification, Issued: 365189050, 365230080, 365233000

File Segment: EPI;
DWPI Class: T01; U13; U14
Manual Codes (EPI/S-X): T01-C07C2; T01-H01D; U13-C04B1A; U13-C04B1B; U13-C04B2; U13-E03; U14-A03B1; U14-A03B4; U14-A03B7; U14-A08B

Latched synchronous output circuit for e.g. cache SRAM for pentium ... ...has latch and parallel slave latch with incoming data inverted by swapping inputs from sense amplifier and sensing data on global bar Alerting Abstract ...The synchronous output buffer device includes a data input terminal, three clock controlled transfer gates, and two **latch** circuits. The first gate (68) is enabled on **one** phase of a **clock cycle** and disabled on another. The second gate is coupled to the output of the first **latch** (75) and has its output coupled to an input terminal of an output driver circuit (95). The third gate is coupled between the input of the first **latch** and an inverted output of the first **latch**. ... ...USE/ADVANTAGE - Also for DRAM, EEPROM and flash EEPROM. High speed output buffer due to clocked parallel operation. Slave **latch** holds input data while additional data is presented for input. **Title Terms** /Index Terms/Additional Words: **LATCH**; Original Publication Data by Authority**Original Abstracts:**The time required to output data from an output buffer is significantly reduced by having a slave **latch** in a parallel **connection** with a **master latch**. Incoming data **is stored** in a **master latch** on a **first phase** of a clock pulse. On the second phase of the clock pulse, the data is output of the **master latch** and provided **to an** output driver. A slave **latch** is coupled to **the** input node of the output driver. On the subsequent phase of the clock, the slave **latch** is **switched** on **to** hold **the** state of the input to the output driver constant. The slave **latch** thus receives the **output** of the **master register** in parallel **with the** output driver and also performs its function of maintaining the input to the output buffer for one entire clock pulse while new data is being presented to the **master latch**. Data is **thus provided** more quickly to the output driver than was previously possible with prior art master/slave configurations. ...**Claims:**data through the transfer gate on a first phase of a clock cycle and disabled on a second phase of the clock cycle;a first **latch** circuit coupled to the output of the **first** transfer gate and receiving the data at the input terminal when the first transfer gate is enabled; anda second clock controlled transfer gate coupled to the output of the first **latch** circuit and having its output coupled to an input **terminal** of an output driver circuit to provide data to the driver circuit from the first **latch** circuit.

33/5,K/3 (Item 3 from file: 350) **Links**
Derwent WPIX

0015499508 *Drawing available*
WPI Acc no: 2006-063646/200607
Related WPI Acc No: 1999-580144; 2000-012972
XRPX Acc No: N2006-055189
Interrupt processing and task switching circuitry for use in computer architectures, has task switching circuit coupled to zero overhead multiplexing circuits for storing later task while simultaneously switching pre-stored earlier task
Patent Assignee: XYRON CORP (XYRO-N)
Inventor: DONOVAN B

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6981133	B1	20051227	US 199738729	P	19970214	200607	B
			US 199823333	A	19980213		
			US 1999410202	A	19990930		

Priority Applications (no., kind, date): US 199823333 A 19980213; US 199738729 P 19970214; US 1999410202 A 19990930

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6981133	B1	EN	13	7	Related to Provisional	US 199738729
					Continuation of application	US 199823333
					Continuation of patent	US 5987601

Alerting Abstract US B1
NOVELTY - A task enable circuit determines whether a predetermined task is ready for execution by CPU, from predetermined inputs. A task priority selection circuit is coupled to output of task enable circuit, for determining an order for running of tasks that are ready. A task switching circuit is coupled to output of selection circuit and zero overhead multiplexing circuit for storing laster task in set of **latches** while simultaneously **switching** pre-stored earlier task.
USE - Interrupt processing and task switching circuitry for use in computer architectures.
ADVANTAGE - Prevents loss of time by eliminating the need to transfer the running task's data to separate task state storage element at the instant of interrupt and task change event. Permits the use of portion of system's task memory for effective tracing of processor flow for full speed, real-time use in computer programming debugging. Allows linking of tasks for mandatory sequential execution of linked tasks as required in multi-tasking systems. Eliminates the need for extensive storage buffers and auxiliary specialized processors with their associated costs and delays. Eliminates the latency involved in long multicycle uninterruptable instructions and latency unpredictability.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of the interrupt processing and task switching circuitry.

Title Terms /Index Terms/Additional Words: INTERRUPT; PROCESS; TASK; SWITCH; CIRCUIT; COMPUTER; COUPLE; ZERO; OVERHEAD; MULTIPLEX; STORAGE; LATE; SIMULTANEOUS; PRE; EARLY

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-009/40			Main		"Version 7"

US Classification, Issued: 712244000, 710264000, 710265000

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F02C; T01-F04

...are ready. A task switching circuit is coupled to output of selection circuit and zero overhead multiplexing circuit for storing laster task in set of **latches** while simultaneously **switching** pre-stored earlier task. Original Publication Data by Authority...**Original Abstracts:**interrupt latency and task change processing overhead delays in computer architectures. Without loss of time, the system performs complete task state saving and restoration between **one cycle** and the **next without** software intervention. For each Central Processing Unit **(1) register**, the invention uses one or **more** auxiliary **latches (3, 4)** wherein one **latch (3, 4)** is used as the "running" **latch** and one of the auxiliary **latches** is attached to **task** storage memory. The invention **swaps connections** between alternate "running" **registers** and auxiliary **registers** while **transferring** other tasks to and **from** task storage **memory (2)**. The invention provides a task linking system to allow the linking of tasks for the mandatory sequential execution of the linked tasks. Further, the... **Claims:**1. In a microprocessor-based computing system having a CPU for executing tasks represented by task **register** sets **and** further including peripheral devices that issue interrupt commands, an interrupt and task change processing circuit comprising:(a) a task enable circuit for determining from predetermined... ... selection circuit, wherein the task switching circuit is coupled to a zero overhead multiplexing circuit for storing a later task in a first set of **latches** during a first clock cycle while simultaneously **switching** a previously stored earlier task stored in **a** second set of **latches** into a task **switch** controller during the **same** clock cycle.

33/5,K/5 (Item 5 from file: 350) **Links**
Derwent WPIX

0014763130 *Drawing available*
WPI Acc no: 2005-110784/200512
XRPX Acc No: N2005-095694
Cyclic redundancy check calculation performing circuit for data communication system, has cyclic redundancy check calculation blocks to perform calculation to yield value of n-bit check result, and check register to latch value
Patent Assignee: BEHERA S (BEHE-I); RIDGEWAY J (RIDG-I); VISWANATH R (VISW-I)
Inventor: BEHERA S; RIDGEWAY J; VISWANATH R

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050005224	A1	20050106	US 2003601175	A	20030619	200512	B

Priority Applications (no., kind, date): US 2003601175 A 20030619

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050005224	A1	EN	9	4	

Alerting Abstract US A1
NOVELTY - The circuit has a set of cyclic redundancy check (CRC) calculation blocks. Each cyclic redundancy check calculation block performs a CRC calculation to yield a value of an n-bit CRC result. A switch **selectively** passes the CRC calculation value. A cyclic redundancy check **register latches** one of the CRC calculation values **selectively** passed by the **switch**. The **latched** value is fedback to the calculation blocks.
DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of calculating a cyclic redundancy check value with a variable width data input.
USE - Used for performing a cyclic redundancy check calculation in a data communication system, and implemented as a field programmable gate array.
ADVANTAGE - The CRC calculation blocks perform the CRC calculation at a short span of time i.e. within **one clock cycle**, thus offering high speed and flexibility. The blocks perform multiple CRC calculations in parallel, hence a cumulative CRC is available from the **register** when required, and is updated every clock cycle.
DESCRIPTION OF DRAWINGS - The drawing shows a flowchart of a method of calculating a cyclic redundancy check value with a variable width data input.

Title Terms /Index Terms/Additional Words: CYCLIC; REDUNDANT; CHECK; CALCULATE; PERFORMANCE; CIRCUIT; DATA; COMMUNICATE; SYSTEM; BLOCK; YIELD; VALUE; N; BIT; RESULT; **REGISTER**; **LATCH**

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
H03M-013/00			Main		"Version 7"

US Classification, Issued: 714758000, 714755000

File Segment: EPI;
DWPI Class: U21; W01
Manual Codes (EPI/S-X): U21-A06A1; U21-C01E; W01-A01B1

...**performing circuit for data communication system, has cyclic redundancy check calculation blocks to perform calculation to yield value of n-bit check result, and check register to latch value Alerting Abstract** ...CRC) calculation blocks. Each cyclic redundancy check calculation block performs a CRC calculation to yield a value of an n-bit CRC result. A switch **selectively** passes the CRC calculation value. A cyclic redundancy check **register latches** one of the CRC calculation values **selectively** passed by the **switch**. The **latched** value is fedback to the calculation blocks. ...ADVANTAGE - The CRC calculation blocks perform the CRC calculation at a short span of time i.e. within **one clock cycle**, thus offering high speed and flexibility. The blocks perform multiple CRC calculations in parallel, hence a cumulative CRC is available from the **register** when required, and is updated every clock cycle... **Title Terms** .../Index Terms/Additional Words: **REGISTER**; **LATCH** Original Publication Data by Authority...**Original Abstracts:**Preferably, multiple CRC calculations are performed in parallel, each CRC calculation involving a different number of data bits from the data word and terminating within **one clock cycle**. The **CRC polynomial is** preferably incorporated into the hardware for each CRC calculation. ...**Claims:**calculation to yield a value of an n-bit CRC result; a switch for selectively passing one of the CRC calculation values; and a CRC **register** for **latching** the one of the CRC calculation values **selectively** passed by the **switch.**

33/5,K/8 (Item 8 from file: 350) **Links**
Derwent WPIX

0013799560 *Drawing available*
WPI Acc no: 2003-899626/200382
XRPX Acc No: N2003-718064
Serial to parallel data converter for high speed serial transmissions, has pre-register that latches parallel data and selector that selects data receivers for serial data conversion and parallel data output, respectively
Patent Assignee: VIA TECHNOLOGIES INC (VIAT-N)
Inventor: CHIANG C

Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20030193424	A1	20031016	US 2002287662	A	20021105	200382	B
TW 541806	A	20030711	TW 2002107481	A	20020412	200406	E
US 6768431	B2	20040727	US 2002287662	A	20021105	200449	E

Priority Applications (no., kind, date): US 2002287662 A 20021105; TW 2002107481 A 20020412

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20030193424	A1	EN	10	5	
TW 541806	A	ZH			

Alerting Abstract US A1
NOVELTY - The converter has two data receivers (10, 20) of n **flip- flops** (11, 21) for **latching** n-bit parallel data. A pre- **register** of m **flip-flops latch** m-bits of the n-bit parallel data and output is connected to the inputs of both the receivers. A **selector** (40) connected to the **flip-flops** of the receivers, **selects** a receiver for serial data conversion and another for parallel data output.
DESCRIPTION - The inputs of the latter data receiver are connected in parallel with that of the former. The inputs of the pre-**register** receive the serial data and the m-bits are shifted back to one of the receivers before each of the conversion cycle ends. The **flip- flops** of both the data receivers are of D-type. An INDEPENDENT CLAIM is also included for a serial to parallel data conversion method.
USE - Used in high-speed serial transmissions.
ADVANTAGE - The converter generates number of phase clocks signals equal to the width of the bits in the parallel data, thereby effectively reducing the number of required clocks and enabling operation at high frequency. The pre-**register** does not need switch control so it does not have the setup time problem during parallel data switching.
DESCRIPTION OF DRAWINGS - The drawing shows a **latch** circuit diagram for serial-to-parallel conversions in **multi**-clock phase architecture.
10, 20 Data receivers
11, 21 **Flip- flops**

40 Selector

Title Terms /Index Terms/Additional Words: SERIAL; PARALLEL; DATA; CONVERTER; HIGH; SPEED; TRANSMISSION; PRE; **REGISTER**; **LATCH**; SELECT; RECEIVE; CONVERT; OUTPUT; RESPECTIVE

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
H03M-009/00			Main		"Version 7"
H03K-005/00			Secondary		"Version 7

US Classification, Issued: 341100000, 341100000, 341101000

File Segment: EPI;
DWPI Class: U21; U22
Manual Codes (EPI/S-X): U21-A05B; U22-A04C

Serial to parallel data converter for high speed serial transmissions, has pre-register that latches parallel data and selector that selects data receivers for serial data conversion and parallel data output, respectively
Alerting Abstract ...NOVELTY - The converter has two data receivers (10, 20) of n **flip -flops** (11, 21) for **latching** n-bit parallel data. A pre- **register** of m **flip-flops latch** m-bits of the n-bit parallel data and output is connected to the inputs of both the receivers. A **selector** (40) connected to the **flip-flops** of the receivers, **selects** a receiver for serial data conversion and another for parallel data output. DESCRIPTION - The inputs of the latter data receiver are connected in parallel with that of the former. The inputs of the pre-**register** receive the serial data and the m-bits are shifted back to one of the receivers before each of the conversion cycle ends. The **flip- flops** of both the data receivers are of D-type. An INDEPENDENT CLAIM is also included for a serial to parallel data conversion method... ...the width of the bits in the parallel data, thereby effectively reducing the number of required clocks and enabling operation at high frequency. The pre-**register** does not need switch control so it does not have the setup time problem during parallel data switching... ...DESCRIPTION OF DRAWINGS - The drawing shows a **latch** circuit diagram for serial-to-parallel conversions in **multi**-clock phase architecture... ...11, 21 **Flip- flops Title Terms** .../Index Terms/Additional Words: **REGISTER**; **LATCH**; Original Publication Data by Authority...**Original Abstracts:**invention can further solve the setup time problem associated with the switching one of two parallel data receivers as the parallel data output. A pre-**register** is employed in **the** converter of the present invention. Since this pre-**register** does not need **switch** control, it does not have the setup time problem during parallel data switching... ... invention can further solve the setup time problem associated with the switching one of two parallel data receivers as the parallel data output. A pre-**register** is employed in the converter of the present **invention**. Since this pre-**register** does not need switch control, it does not **have** the setup time problem during parallel data switching. ...**Claims:**A serial-to-parallel data converter for converting a serial data into a n-bit parallel data, comprising:a first data receiver, composed of n **flip-flops** for **latching** the n-bit parallel data;a **second data receiver**, composed **of** n **flip-flops** with inputs connected in parallel **with** inputs of the first data **receiver, for latching** the n-bit parallel data;a pre-**register**, composed of m **flip-flop**(s) for **latching** the first m bit(s) of **the** n-bit parallel **data and** output(s) **thereof** connected to the inputs of **flip-flops** in the first data receiver and the **second** data receiver corresponding to the **first m** bit(s); wherein the inputs of the **pre-register** receive the serial data, and the first m bit(s) is shifted back to **one** of the first data receiver and the second data receiver before each conversion

cycle ends; anda **selector**, connected to the **flip-flops** of the first data receiver and the **second** data receiver for **selecting** one of the **first data** receiver and the **second** data receiver for **serial** data conversion and the other for parallel data output... ... A serial-to-parallel data converter for converting a serial data into a n-bit parallel data, comprising:a first data receiver, composed of n **flip-flops** for **latching** the n-bit parallel data referring n phase clock signals in a conversion cycle;a **second** data receiver, composed of n **flip-flops** with inputs connected **in parallel** with **inputs** of the first data receiver, for **latching** the n-bit parallel data by referring said n phase **clock** signals in said conversion cycle;**a pre-register**, composed of m **flip-flop**(s) for **latching** the first m bit(s) of the n-bit parallel data and output(s) thereof connected to the inputs of **flip-flops** in the first **data** receiver and the **second data** receiver corresponding **to** the first m bit(s); wherein the inputs of the pre-**register** receive the serial data, and the first m **bit(s)** is shifted back to one of the **first** data receiver and the second data receiver before each conversion cycle ends; anda **selector, connected** to the **flip-flops** of the first data receiver and the **second** data receiver for selecting one of the first data receiver and the second data receiver for serial data conversion and the other **for** parallel data output.

33/5,K/11 (Item 11 from file: 350) **Links**
Derwent WPIX

0013213784 *Drawing available*
WPI Acc no: 2003-298326/200329
Related WPI Acc No: 2002-162597
XRPX Acc No: N2003-237194
Memory cell structure for field programmable gate array, has several flip flops with data, clock inputs coupled to respective inputs of shift register and data output coupled to single data bit input of memory cells
Patent Assignee: XILINX INC (XILI-N)
Inventor: GHIA A V; MENON S M; RAU P

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6501677	B1	20021231	US 199830616	A	19980225	200329	B
			US 2001825757	A	20010403		

Priority Applications (no., kind, date): US 199830616 A 19980225; US 2001825757 A 20010403

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 6501677	B1	EN	31	15	Division of application	US 199830616
					Division of patent	US 6222757

Alerting Abstract US B1
NOVELTY - A shift **register** has a chain of **flip-flops**, where clock input of each **flip flop** is coupled to clock input of shift **register** and data input of specific **flip-flop** is coupled to data input of shift **register**. Data output of each **flip-flop** is coupled to single data bit input of a **selective** data path forming unit of memory cells.
USE - For storing programming bits in static RAM-based field programmable gate array (FPGA).
ADVANTAGE - As the **flip-flops** of all the memory bytes for logic block are coupled together in shift-**register**, the need for regularity in the array structure is eliminated, such that there is no need to place the logic blocks in the interstices of memory array. By changing the ROM in a simple manner, functionality can be change from the **one** power up **cycle** to another, thus design changes in the FPGA is made easier, cheaper and faster, thereby enhances and speeds up design cycles.
DESCRIPTION OF DRAWINGS - The figure shows a circuit diagram of the SRAM control memory for FPGA.

Title Terms /Index Terms/Additional Words: MEMORY; CELL; STRUCTURE; FIELD; PROGRAM; GATE; ARRAY; FLIP; DATA; CLOCK; INPUT; COUPLE; RESPECTIVE; SHIFT; **REGISTER**; OUTPUT; SINGLE; BIT

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G11C-011/00			Main		"Version 7"

US Classification, Issued: 365154000, 365189120, 365189050

File Segment: EPI;
DWPI Class: U13; U14
Manual Codes (EPI/S-X): U13-C04B1B; U13-C04D; U13-E04; U14-A07C

Memory cell structure for field programmable gate array, has several flip flops with data, clock inputs coupled to respective inputs of shift register and data output coupled to single data bit input of memory cells
Alerting Abstract ...NOVELTY - A shift **register** has a chain of **flip- flops**, where clock input of each **flip flop** is coupled to clock input of shift **register** and data input of specific **flip-flop** is coupled to data input of shift **register**. Data output of each **flip-flop** is coupled to single data bit input of a **selective** data path forming unit of memory cells. ...ADVANTAGE - As the **flip-flops** of all the memory bytes for logic block are coupled together in shift-**register**, the need for regularity in the array structure is eliminated, such that there is no need to place the logic blocks in the interstices of memory array. By changing the ROM in a simple manner, functionality can be change from the **one** power up **cycle** to another, thus design changes in the FPGA is made easier, cheaper and faster, thereby enhances and speeds up design cycles... **Title Terms** .../Index Terms/Additional Words: **REGISTER**; Original Publication Data by Authority...**Original Abstracts:**FPGA eliminates the need for a regular array of word lines and bit lines. The memory includes memory bytes, each of which has eight SRAM **latches**, a single **flip-flop** and a **one-of**-eight decoder having data input coupled to the inverting output of the **flip-flop** and eight **individual data** outputs, each of which is coupled to a data input of one of the SRAM **latches**. The **flip-flops of** all **memory bytes** for a logic block are coupled together in a serpentine shift **register**. Loading of configuration **data** involves shutting down all paths through the decoder, shifting all configuration bits for the "0" position SRAM **latch** of each memory **byte** into the shift **register**, and setting the **address** bits to the decoder so as to create a conductive path on each memory byte from the output of the **flip-flop** to the **data input** of the 0 **latch**. The process is **then** repeated for the seven other SRAM **latch** positions. ...**Claims:**data bit input and one of said plurality of outputs depending on the address bits received at said address input; andat least one shift **register** having a data input and a clock input, for receiving at said **data** input a string of data bits in serial format which are shifted into said shift **register** in accordance with clock signals received at said clock input, said shift **register** comprising a chain of **flip-flops**, each **flip-flop** having a clock **input**, a data input, and **at least** one **data output**, wherein the clock input of each **flip-flop** is coupled to the clock input of said shift **register**; the **data input** of one **flip-flop** in the chain is coupled **to** the data input of said **shift register**; the data input of every **flip-flop** other than said one is **coupled** to a data output of **the previous flip-flop** in said chain; and a data output of each **flip-flop is coupled** to the single data bit input of the **selective data path** forming means of one of said groups of memory cells.

33/5,K/15 (Item 15 from file: 350) **Links**
Derwent WPIX

0010313571 *Drawing available*
WPI Acc no: 2000-627688/200060
XRPX Acc No: N2000-465033
Extended mode transfer instruction speed-up apparatus, has selector that selects absolute address from adder and main address generator, when control signals are in predetermined state
Patent Assignee: UNISYS CORP (BURS)
Inventor: JOHNSON D C; LUCAS G J

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6081881	A	20000627	US 199826935	A	19980220	200060	B

Priority Applications (no., kind, date): US 199826935 A 19980220

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6081881	A	EN	11	6	

Alerting Abstract US A
NOVELTY - Selector (2-6) selects any one of the control signals generated corresponding to predetermined transfer instructions. A **latching** unit **latches** the **selected** control signal into base **register** (4-6). When the signal changes state. Another selector (8-6) selects absolute value from an adder (6-6) and from main address generator (82A), when the control signals are in their respective state.
DESCRIPTION - A testing unit determines whether current instruction is one of predetermined transfer instructions. The first control signal showing state of presence of the transfer instruction is output by an output unit. The base address stored in base **register** (4-6) of current instruction is added to offset provided by current instruction for generating absolute address by an adder. If the state of first control signal changes, another control signal having state similar to that of first control signal, is generated.
USE - For general purpose digital data processing system.
ADVANTAGE - Reduces response and computation time of extended mode transfer instructions in predetermined time for certain selected transfer instructions.
DESCRIPTION OF DRAWINGS - The figure shows the block diagram of added instruction cache generator.
2-6,8-6 Selectors
4-6 Base **register**
6-6 Adder
82A Address generator

Title Terms /Index Terms/Additional Words: EXTEND; MODE; TRANSFER; INSTRUCTION; SPEED; UP; APPARATUS; SELECT; ABSOLUTE; ADDRESS; ADDER; MAIN; GENERATOR; CONTROL; SIGNAL;

PREDETERMINED; STATE

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-012/00			Main		"Version 7"

US Classification, Issued: 711220000, 711002000

File Segment: EPI;
DWPI Class: T01; U21
Manual Codes (EPI/S-X): T01-F03A; U21-C03A1; U21-C03B2

Alerting Abstract ...NOVELTY - Selector (2-6) selects any one of the control signals generated corresponding to predetermined transfer instructions. A **latching** unit **latches** the **selected** control signal into base **register** (4-6). When the signal changes state. Another selector (8-6) selects absolute value from an adder (6-6) and from main address generator (82A... ...instructions. The first control signal showing state of presence of the transfer instruction is output by an output unit. The base address stored in base **register** (4-6) of current instruction is added to offset provided by current instruction for generating absolute address by an adder. If the state of first... ...4-6 Base **register** Original Publication Data by Authority...**Original Abstracts:**a fast transfer is possible. The fast transfer process requires fewer checks than the previous apparatus which accelerates the response to selected transfer instructions by **one cycle.** ...**Claims:**first control signal with a second state; c) adder means for generating an absolute first address by adding the base address stored in the base **register** of the current instruction to an offset **also** provided by the current instruction; d) means for generating a second control signal, which changes state, **one** memory **cycle** after the first control signal changes state, **to** the **same** state as the first control signal; e) first selection means for selecting a first value when the first control signal is in the first state, and selecting a second value when the first control signal is in the second state; f) **latching** means for **latching** the first **selection** means **selection** into the base **register** whenever **the** first control **signal** changes state; g) second **selection** means for **selecting the** absolute value from the adder means when the second control signal is in the first state and for selecting the absolute value from the main...

33/5,K/18 (Item 18 from file: 350) **Links**
Derwent WPIX

0009629155 *Drawing available*
WPI Acc no: 1999-580144/199949
Related WPI Acc No: 2000-012972; 2006-063646
XRPX Acc No: N1999-428324
Zero overhead computer interrupts circuit with task switching used in computer architectures
Patent Assignee: GILLETTE CO (GILL); XYRON CORP (XYRO-N)
Inventor: DONOVAN B; FALAHERTY P; GERALD T S; GUAY M J; METCALF S C

Patent Family (17 patents, 84 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1999041661	A1	19990819	WO 1999US2575	A	19990205	199949	B
AU 199926598	A	19990830	AU 199926598	A	19990205	200003	E
NO 200004043	A	20001011	WO 1999US2575	A	19990205	200063	E
			NO 20004043	A	20000811		
EP 1062572	A1	20001227	EP 1999906765	A	19990205	200102	E
			WO 1999US2575	A	19990205		
CN 1293776	A	20010502	CN 1999803977	A	19990205	200143	E
KR 2001040959	A	20010515	KR 2000708888	A	20000814	200167	E
JP 2002503845	W	20020205	WO 1999US2575	A	19990205	200212	E
			JP 2000531779	A	19990205		
TW 448366	A	20010801	TW 1999102041	A	19990210	200222	E
BR 199907848	A	20020507	BR 19997848	A	19990205	200238	E
			WO 1999US2575	A	19990205		
MX 2000007850	A1	20020901	WO 1999US2575	A	19990205	200370	E
			MX 20007850	A	20000811		
MX 218567	B	20040108	WO 1999US2575	A	19990205	200472	E
			MX 20007850	A	20000811		
CN 1116639	C	20030730	CN 1999803977	A	19990205	200548	E
IN 200000265	P2	20050923	WO 1999US2575	A	19990205	200623	E
			IN 2000KN265	A	20000828		
IN 200000265	P1	20051125	WO 1999US8609	A	19990420	200639	E
			IN 2000DN265	A	20001017		
KR 2006024029	A	20060315	WO 1999US2575	A	19990205	200668	E
			KR 2006703806	A	20060224		
KR 2006031883	A	20060413	WO 1999US2575	A	19990205	200674	E
			KR 2006703804	A	20060224		
KR 617357	B1	20060828	WO 1999US2575	A	19990205	200714	E
			KR 2000708888	A	20000814		

Priority Applications (no., kind, date): US 199823333 A 19980213; US 199866499 A 19980424

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1999041661	A1	EN	26	7		
National Designated States,Original	AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 199926598	A	EN			Based on OPI patent	WO 1999041661
NO 200004043	A	NO			PCT Application	WO 1999US2575
EP 1062572	A1	EN			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
JP 2002503845	W	JA	26		PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
TW 448366	A	ZH				
BR 199907848	A	PT			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
MX 2000007850	A1	ES			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
MX 218567	B	ES			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
IN 200000265	P2	EN			PCT Application	WO 1999US2575
IN 200000265	P1	EN			PCT Application	WO 1999US8609
KR 2006024029	A	KO			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
KR 2006031883	A	KO			PCT Application	WO 1999US2575
					Based on OPI patent	WO 1999041661
KR 617357	B1	KO			PCT Application	WO 1999US2575
					Previously issued patent	KR 2001040959
					Based on OPI patent	WO 1999041661

Alerting Abstract WO A1

NOVELTY - Multiplexers (14,15) having inputs from the central processing unit (CPU) (1) and task storage memory (2) are each connected to auxiliary **latches** (3,4). Additional multiplexers have inputs from each **latch**, one (13) connecting to an input of the task storage memory and one (17), the "running" **latch**, connecting to the CPU. Connections are **exchanged** between **alternate** "running" **registers** and auxiliary **registers** while transferring other

tasks to and from task storage memory.
USE - The system is used in computer architectures.
ADVANTAGE - The system allows the mandatory sequential execution of linked tasks and provides a counter to increase priorities of various tasks as their deadline approaches. Delays and costs are reduced by eliminating storage buffers and specialized processors. A deterministic architecture structure is created.
DESCRIPTION OF DRAWINGS - The figure shows a circuit diagram of an interrupt and task exchange system.
1 Central processing unit
2 Task storage memory
3,4 Auxiliary **latches**
13,14,15,17 Multiplexers

Title Terms /Index Terms/Additional Words: ZERO; OVERHEAD; COMPUTER; INTERRUPT; CIRCUIT ; TASK; SWITCH

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
B26B-021/40; G06F; G06F-013/26; G06F-009/30; G06F-009/40; G06F-009/46			Main		"Version 7"
G06F-0009/30	A	I	F	B	20060101
G06F-0009/30	A	I	F	V	20060101
G06F-0009/40	A	I	F	B	20060101
G06F-0009/46	A	I		R	20060101
G06F-0009/48	A	I	F	B	20060101
G06F-0009/48	A	I	L	R	20060101
G06F-0009/46	C	I	F	B	20060101
G06F-0009/46	C	I		R	20060101
G06F-0009/30	C	I	F	B	20060101

File Segment: EngPI; EPI;
DWPI Class: T01; P62
Manual Codes (EPI/S-X): T01-F02A1; T01-F04; T01-H05B1

Alerting Abstract ...NOVELTY - Multiplexers (14,15) having inputs from the central processing unit (CPU) (1) and task storage memory (2) are each connected to auxiliary **latches** (3,4). Additional multiplexers have inputs from each **latch**, one (13) connecting to an input of the task storage memory and one (17), the "running" **latch**, connecting to the CPU. Connections are **exchanged** between **alternate** "running" **registers** and auxiliary **registers** while transferring other tasks to and from task storage memory. ...3,4 Auxiliary **latches** Original Publication Data by Authority...**Original Abstracts:**interrupt latency as task change processing overhead delays in computer architectures. Without loss of time, the system performs complete task state saving and restoration between **one cycle** and the next without software intervention. For each Central Processing Unit (1) the invention uses one or more auxiliary **latches** (3, 4) wherein one **latch** (4) is used as the "running" **latch** and one of the auxiliary **latches** is attached to task storage memory. The invention **swaps** connections between alternate "running" **registers** and

auxiliary **registers** while transferring other tasks to and from task storage memory (2). The invention provides a task linking system to allow the linking of tasks for... ... interrupt latency as task change processing overhead delays in computer architectures. Without loss of time, the system performs complete task state saving and restoration between **one cycle** and the next without software intervention. For each Central Processing Unit (1) the invention uses one or more auxiliary **latches** (3, 4) wherein one **latch** (4) is used as the "running" **latch** and one of the auxiliary **latches** is attached to task storage memory. The invention **swaps** connections between alternate "running" **registers** and auxiliary **registers** while transferring other tasks to and from task storage memory (2). The invention provides a task linking system to allow the linking of tasks for...

33/5,K/29 (Item 29 from file: 350) **Links**
Derwent WPIX

0006630899 *Drawing available*
WPI Acc no: 1994-007027/199401
XRPX Acc No: N1994-005804
Digital data processor executing conditional instruction within single machine cycle - has two temporary registers for holding two pieces of data read from two general registers specified by instruction, to provide architecture for pipeline processing
Patent Assignee: FUJI XEROX CO LTD (XERF)
Inventor: KAWATA T

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5274777	A	19931228	US 1991676692	A	19910329	199401	B

Priority Applications (no., kind, date): JP 199088483 A 19900403

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5274777	A	EN	9	6	

Alerting Abstract US A
The digital data processor includes a CPU, and a memory from which a condition instruction is fetched and passed to an instruction **register**. A first control circuit responds to source-codes to select the general **registers** having respective pieces of data to be compared. A first **latch** stores instruction data including a code for an operation to be performed by an arithmetic and logic unit (ALU) on the two pieces of data under the control of a second control circuit.
A conditional code **register** stores a conditional code representing the result of the ALU operation, and a **second latch** stores **selection** criteria for destination **registers** specified by the instruction. A selection circuit operates under the control of a third control circuit to sort the ALU output data of a third control circuit to the specific destination **register** in accordance with the selection criteria and the condition code.
ADVANTAGE - Allows pipeline processing to be performed without disturbance or processing time penalty, which ensures high-speed performance. Instruction execution is completed within a **single** CPU **cycle**.

Title Terms /Index Terms/Additional Words: DIGITAL; DATA; PROCESSOR; EXECUTE; CONDITION ; INSTRUCTION; SINGLE; MACHINE; CYCLE; TWO; TEMPORARY; **REGISTER**; HOLD; PIECE; READ; GENERAL; SPECIFIED; ARCHITECTURE; PIPE; PROCESS

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date

38/5,K/7 (Item 7 from file: 350) **Links**
Derwent WPIX

0009039188 *Drawing available*
WPI Acc no: 1998-597086/199851
XRPX Acc No: N1998-464693
Expandable dynamic random access memory - has motherboard with memory control unit which generates row and column addresses as function of memory configuration, memory address and read/write command
Patent Assignee: BULL HN INFORMATION SYSTEMS ITAL SPA (HONE)
Inventor: GIANELLINI M; LAZZARI A

Patent Family (2 patents, 24 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 880142	A1	19981125	EP 1997830231	A	19970520	199851	B
US 6170035	B1	20010102	US 199880991	A	19980519	200103	E

Priority Applications (no., kind, date): EP 1997830231 A 19970520

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
EP 880142	A1	EN	15	6	
Regional Designated States,Original	AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC NL PT RO SE SI				

Alerting Abstract EP A1
The dynamic random access memory (DRAM) includes a motherboard (60). A memory control unit (5) is mounted on the motherboard in order to configure the memory and to generate, as a function of the memory configuration, of a memory address and of a read/write command received via a system bus (6). A row address (RADDR) and a column address (COL.ADDR) are placed at successive time intervals on an address output channel (17). A pair of **several** distinct timed signals (RAS.XY, CAS.XY. X=A,B,C,D,. Y=0,1-5) validate row and column addresses respectively, **selectively** directed to one and only one of the modules. One of **several** distinct timed write commands WE(0-5) and one of **several** distinct **latch** commands ALE(0-5) for the column address are **selectively** directed to one and only one of the memory blocks.
A first group of connection slots (13-16) are mounted on the motherboard and interconnected with the memory control unit in order to receive, the row and column addresses, the write commands, the **latch** commands and the timed signals to validate row and column addresses. One or more memory components of the same type are inserted in the slots. The type is either memory modules (1-4) of commercial DIMM type or supports (62) for memory modules of commercial DIMM type. The support includes a printed circuit board (37) with edge connector (38) insertion into a slot of the first group. A second group of connection slots (39-44) for memory modules of DIMM type. At least one memory module of DIMM type is plugged into a slot of the **second** group and **several latch registers** (45-50) each associated with a slot of the **second** group. Each **register** is controlled by one of the **latch** commands to **latch** the column address received through the edge connector and present it to address terminals of the associated slot.

ADVANTAGE - Allows expansion of memory using non-interleaved DIMM modules connected directly to slots in motherboard.

Title Terms /Index Terms/Additional Words: EXPAND; DYNAMIC; RANDOM; ACCESS; MEMORY; CONTROL; UNIT; GENERATE; ROW; COLUMN; ADDRESS; FUNCTION; CONFIGURATION; READ; WRITING; COMMAND

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-012/00; G11C-007/00			Main		"Version 7"
G11C-005/00			Secondary		"Version 7

US Classification, Issued: 711005000, 711105000, 711002000

File Segment: EPI;
DWPI Class: T01; U13; U14; V04
Manual Codes (EPI/S-X): T01-H01B3; U13-C04B1A; U14-A; U14-A03B4; U14-A07; V04-Q02B

Alerting Abstract ...A row address (RADDR) and a column address (COL.ADDR) are placed at successive time intervals on an address output channel (17). A pair of **several** distinct timed signals (RAS.XY, CAS.XY. X=A,B,C,D,. Y=0,1-5) validate row and column addresses respectively, **selectively** directed to one and only one of the modules. One of **several** distinct timed write commands WE(0-5) and one of **several** distinct **latch** commands ALE(0-5) for the column address are **selectively** directed to one and only one of the memory blocks... ...are mounted on the motherboard and interconnected with the memory control unit in order to receive, the row and column addresses, the write commands, the **latch** commands and the timed signals to validate row and column addresses. One or more memory components of the same type are inserted in the slots... ...connection slots (39-44) for memory modules of DIMM type. At least one memory module of DIMM type is plugged into a slot of the **second** group and **several latch registers** (45-50) each associated with a slot of the **second** group. Each **register** is controlled by one of the **latch** commands to **latch** the column address received through the edge connector and present it to address terminals of the associated slot... Original Publication Data by Authority...**Original Abstracts:**random access memory (DRAM) with variable configuration depending on the number and capacity of standard memory modules, of DIMM type (1) plugged into a first **plurality** of slots (13, **14**, 15, 16) of a memory motherboard (61) comprising a control unit (5), into which it is possible to plug, into the first **plurality** of slots (13, **14**, 15, 16), in **substitution** for the memory **modules** (1), expansion supports (62) (Memory Riser), in turn provided with - a second **plurality** of slots (39, **40**, 41, 42, 43, 44) for the insertion of standard memory modules of DIMM type (1), - and of column address **latch registers** (45, 50) **each associated** with a slot of the **second plurality** and thereby **to support** and allow the configurability and operability of interleaved-block memory, and access **cycles**, with partial time **overlap**,without renouncing the use of commercially available DIMM memory modules and without burdening the basic memory configuration with all the overheads required to support the... ... Dynamic random access memory with variable configuration depending on the number and capacity of standard memory modules, of DIMM type plugged into a first **plurality** of slots of a **memory** motherboard comprising a control unit, into which it is possible to plug, into the first **plurality** of slots, in **substitution for** the memory modules, **expansion** supports, in turn provided with a second **plurality** of slots for the **insertion** of standard memory modules of DIMM type, and of

G06F-007/36			Main		"Version 7"
G06F-007/08			Secondary		"Version 7

US Classification, Issued: 395375000, 395600000, 364DIG001, 364222900, 364271600, 364271800, 364231800, 364962300

File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-F03

Digital data processor executing conditional instruction within single machine cycle - ... ...has two temporary registers for holding two pieces of data read from two general registers specified by instruction, to provide architecture for pipeline processing Original Titles: Digital data processor executing a conditional instruction within a **single** machine **cycle Alerting Abstract** ...The digital data processor includes a CPU, and a memory from which a condition instruction is fetched and passed to an instruction **register**. A first control circuit responds to source-codes to select the general **registers** having respective pieces of data to be compared. A first **latch** stores instruction data including a code for an operation to be performed by an arithmetic and logic unit (ALU) on the two pieces of data... ...A conditional code **register** stores a conditional code representing the result of the ALU operation, and a **second latch** stores **selection** criteria for destination **registers** specified by the instruction. A selection circuit operates under the control of a third control circuit to sort the ALU output data of a third control circuit to the specific destination **register** in accordance with the selection criteria and the condition code... ...ADVANTAGE - Allows pipeline processing to be performed without disturbance or processing time penalty, which ensures high-speed performance. Instruction execution is completed within a **single** CPU **cycle. Title Terms** .../Index Terms/Additional Words: **REGISTER**; Original Publication Data by Authority**Original Abstracts:** In a digital data processor having a CPU, a condition instruction is fetched from memory to an instruction **register**. A first control **circuit** responds to source-codes to select the general **registers having** respective pieces **of** data to be compared. A first **latch** stores instruction data **including** a code for an operation to be performed by an arithmetic and logic unit (ALU) on the two pieces of data under the control of a second control circuit. A conditional code **register** stores a conditional **code**. representing the result of the ALU operation, and a **second latch** stores **selection** criteria **for** destination **registers** specified by the **instruction**. A **selection** circuit operates under the control of a third control circuit to sort the ALU output data of a third control circuit to the specific destination **register** in accordance with **the** selection criteria and the condition code. The instruction execution is completed within a **single** CPU **cycle.** ...**Claims:**processor having a central processing unit operating in response to a stored set of instruction, a basic instruction of said instructions being executed within a **single** machine **cycle**, said **digital** processor comprising: an instruction **register** for **reading** an instruction; a plurality of general **registers** for **storing** data; means for reading respective pieces of data from two of said plurality of general **registers**, said **two** general **registers** being **specified** by instruction; operation means for applying an operation specified by the instruction to said pieces of data supplied from said general **registers**; means **for** generating a conditional code from the operated data produced by said operation means; means for selecting one of said respective pieces of data from said... ... of data is larger or smaller than the other of said respective pieces of data as specified by the instruction, and for selecting a general **register** being **specified** by the instruction as a destination for the selected piece of data; and means for controlling said general **registers**, said **operation** means, said condition code generating means, said reading means, and said selecting means so that the instruction is executed within a **single** machine **cycle.**

column address **latch registers** each associated with **a slot** of the **second plurality** and thereby to **support and** allow the configurability and operability of interleaved-block memory, and access **cycles**, with partial time overlap, **without** renouncing the use of commercially available DIMM memory modules and without burdening the basic memory configuration with all the overheads required to support the interleaved... ...**Claims:**a row address (RADDR) and a column address (COL.ADDR) placed at successive time intervals on an address output channel (17), a pair of a **plurality** of distinct timed **signals** (RAS.XY, CAS.XY; X=A,B,C,D,; Y=0,1...5) validating row and column addresses respectively, **selectively** directed to one **and** only one of said modules, one of a **plurality** of distinct timed **write** commands WE(0...5) and one of a **plurality** of distinct **latch commands** ALE(0...**5**) for said column address, **selectively** directed to one **and** only one of the said memory blocks, - a first **plurality** of connection slots (13, **14**, 15, 16) mounted on said motherboard and interconnected with said memory control unit (5) in order to receive, from said memory control unit, said row and column addresses, said write commands WE(0...5), said **latch** commands ALE(0...5) **and** said **plurality** of timed signals for **validating** row and column addresses and, inserted in said slots - one or more memory components of the same type, **chosen** from the following two types: - **memory** modules (1, 2, 3, 4) of commercial DIMM type - supports (62) for memory modules of commercial DIMM type comprising a printed circuit board (37) with edge connector (38) for insertion into a slot (13, 14, 15, 16) of said first **plurality**, a second **plurality** of connection slots (39...**44**) for memory **modules** of DIMM type, at least one memory module of DIMM type plugged into a slot of the said **second** plurality and a **plurality** of **latch** registers (**45**...**50**) each associated **with** a **slot of** said **second** plurality, each controlled by one of said **latch commands** ALE(0...5) for **latching** said **column** address received through said edge **connector** (38) and for presenting it to address terminals of the associated slot... ... via a system bus, a row address and a column address placed at successive time intervals on an address output channel, a pair of a **plurality** of distinct timed signals validating row and column addresses respectively, **selectively** directed to one and **only** one of said modules, one of a **plurality** of distinct **timed** write commands and one of a **plurality** of distinct **latch** commands for **said** column address, **selectively** directed to one and only one **of** the said **memory** blocks, a first **plurality** of **connection** slots mounted on said motherboard and interconnected with said memory control unit in order to **receive**, from said memory control unit, said row and column addresses, said write commands, said **latch** commands and said **plurality** of timed signals for validating row and column addresses and, inserted in said **slots**, one or more **memory** components of the same type, **chosen** from the following two types: memory modules of commercial DIMM type, and expansion supports for memory modules of commercial **DIMM** type, each expansion slot comprising a printed circuit board with an edge connector for insertion into a slot of said first **plurality**, a second **plurality** of connection slots for memory modules of DIMM type, at least one memory module of DIMM type plugged into a **slot** of the **said** second **plurality** and a **plurality** of **latch registers** each associated with a slot of said **second plurality**, each controlled by one of said **latch commands for latching** said **column** address **received through** said edge connector and for presenting it **to address** terminals of the associated slot.

38/5,K/12 (Item 12 from file: 350) **Links**
Derwent WPIX

0006813805 *Drawing available*
WPI Acc no: 1994-201292/199425
XRPX Acc No: N1994-158330
Delay circuitry variable while operating - stores discrete signal samples at intervals determined by clock signal in sequence in chain of memory elements
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NV (PHIG); PHILIPS GLOEILAMPENFAB NV (PHIG); PHILIPS PATENTVERWALTUNG GMBH (PHIG); US PHILIPS CORP (PHIG)
Inventor: SUWALD T

Patent Family (7 patents, 7 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
DE 4242201	A1	19940616	DE 4242201	A	19921215	199425	B
EP 607630	A1	19940727	EP 1993203471	A	19931210	199429	E
JP 6237157	A	19940823	JP 1993313393	A	19931214	199438	E
US 5554949	A	19960910	US 1993167265	A	19931214	199642	E
EP 607630	B1	19990317	EP 1993203471	A	19931210	199915	E
DE 59309461	G	19990422	DE 59309461	A	19931210	199922	E
			EP 1993203471	A	19931210		
KR 296208	B	20011024	KR 199327735	A	19931215	200236	E

Priority Applications (no., kind, date): DE 4242201 A 19921215

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
DE 4242201	A1	DE	10	3		
EP 607630	A1	DE	12	4		
Regional Designated States,Original	DE FR GB IT					
JP 6237157	A	JA	9			
US 5554949	A	EN	9	3		
EP 607630	B1	DE				
Regional Designated States,Original	DE FR GB IT					
DE 59309461	G	DE			Application	EP 1993203471
					Based on OPI patent	EP 607630
KR 296208	B	KO			Previously issued patent	KR 94017157

Alerting Abstract DE A1
The delay circuit stores discrete signal samples at intervals determined by a clock signal (CL) in sequence in a chain

of memory elements to provide a predefined delay time. Each memory element operates a driving device.
A shift **register** arrangement is formed from a chain of time-base circuits (20). Each driving device includes one of the time-base circuits. All time-base circuits are **switched** by the clock signal. A control arrangement supplies a start pulse to the first time-base circuit at a first time, t1. The start pulse is passed through the shift **register** arrangement until a second time, t2. The time between t1 and t2 is a **selectable** whole number of the period of the **clock cycle**.
ADVANTAGE - Can be adapted, pref. **switched**, to provide **multiple** different delay times in simple way.

Title Terms /Index Terms/Additional Words: DELAY; CIRCUIT; VARIABLE; OPERATE; STORAGE; DISCRETE; SIGNAL; SAMPLE; INTERVAL; DETERMINE; CLOCK; SEQUENCE; CHAIN; MEMORY; ELEMENT

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
H03H-011/26; H03K-005/00; H03K-005/135			Main		"Version 7"
G11C-027/04; H03H-017/08; H03K-001/04; H03K-017/28			Secondary		"Version 7

US Classification, Issued: 327276000, 327279000, 327291000, 327293000, 327294000, 327400000, 327401000

File Segment: EPI;
DWPI Class: U22; W04
Manual Codes (EPI/S-X): U22-D04; W04-P01N

Alerting Abstract ...A shift **register** arrangement is formed from a chain of time-base circuits (20). Each driving device includes one of the time-base circuits. All time-base circuits are **switched** by the clock signal. A control arrangement supplies a start pulse to the first time-base circuit at a first time, t1. The start pulse is passed through the shift **register** arrangement until a second time, t2. The time between t1 and t2 is a **selectable** whole number of the period of the **clock cycle**. ... ...ADVANTAGE - Can be adapted, pref. **switched**, to provide **multiple** different delay times in simple way. Original Publication Data by Authority...**Original Abstracts:**output circuit (13) of the memory arrangement (11) following in the series, by in each case one actuating device (14, 15, 20), comprising a shift **register arrangement** formed from a chain of bistable **flipflop circuits** (20),in which arrangement the output (25) of in each case one of the **flipflop circuits** (20) is connected to the input of the following **flipflop circuit** (20) in the chain, each actuating device (14, 15, 20) comprises in each case one of the **flipflop circuits** (20) and all **flipflop circuits** (20) are **switched by** the clock signal (CL), and comprising a command arrangement (35) which, at a first time (t1) supplies a (first) start pulse (ST) to the first **flipflop circuit** (20) in the shift **register arrangement** and enables the shift **register arrangement** for forwarding the start pulse (ST) through the chain of **flipflop circuits** (20) as determined by the clock signal (CL), and which interrupts the forwarding of the (first) start pulse (ST) at a second time (t10) and, at the same time,supplies a next start pulse (ST) to the first **flipflop circuit** (20) in the shift **register arrangement** and again enables the shift **register arrangement** for forwarding this next start pulse (ST), the time interval between the first (t1) and the second (t10) time being a **selectable integral multiple of** periods of the clock signal (CL) and the number (n) of the memory arrangements (11) or respectively of the **flipflop circuits** (20) corresponding at least to this **multiple** (**n**) of the periods of the clock signal (CL). In operation, this circuit arrangement can be adapted in a simple manner to a **multiplicity** of **different** values for the desired delay time... ...

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Set     Items   Postings   Description
S1     188818     300203   S REGISTER?
S2      35539     122409   S LATCH? OR LATCH()VALVE? OR FLIPFLOP? OR FLIP()FLOP? ?
S3       2484      14815   S S1 AND S2
S4        232        331   S PRIMARY OR MAIN OR 1ST OR MASTER OR PRINCIPAL
S5        249        360   S SELECT? OR CHOOS? OR CHOIC? OR CHOSE?
S6        245        380   S ASSIGN? OR PICK? OR DESIGNAT? OR ELECT???
S7          0          0   S OPT OR OPTS OR OPTING OR OPTED
S8        745       1426   S PLURAL? OR MULTI OR MULTIPLE OR MULTIPLICIT? OR MULTITUD? OR
SEVERAL? OR NUMEROUS? OR MANY OR ARRAY
S9        305        473   S SECOND? OR 2ND OR ALTERNAT? OR BACKUP? OR SLAVE OR REDUNDAN?
S10       965       1789   S SINGLE OR ONE OR UNIQUE? OR SPECIFIC OR PARTICULAR OR SOLE
S11       217        555   S CLOCK()CYCLE? OR CYCLE? OR CLOCKCYCL? OR CLOCK()INTERVAL?
S12       418        922   S SWAP? OR TRADE? OR TRADING? OR SWITCH??? OR INTERCHANG? OR
SUBSTITUT?
S13        16         35   S EXCHANG? OR SUPPLANT? OR SUPERCED? OR SUPERCESS?
S14         2          3   S MULTITHREAD? OR (MULTI OR MULTIPLE OR MULTIPLICIT? OR
MULTITUD? OR SEVERAL? OR NUMEROUS? OR MANY OR ARRAY)(2W)THREAD?
S15       232       2097   S S3 AND (S4 OR S8:S9) AND S5:S7
S16        62        711   S S15 AND S12
S17         5         43   S S15 AND S10(5N)S11
S18        34        294   S S3 AND S10(5N)S11
S19        96       1031   S S16:S18
S20        76        889   S S19 AND PY=1970:2003
S21        80        848   S S19 NOT PY=2004:2007
S22        80       1172   S S20:S21
S23        50        760   RD  (unique items)
 ; show files
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[File 2] **INSPEC** 1898-2007/Jul W4

[File 6] **NTIS** 1964-2007/Jul W5

[File 8] **Ei Compendex(R)** 1884-2007/Jul W3

[File 34] **SciSearch(R) Cited Ref Sci** 1990-2007/Jul W5

[File 35] **Dissertation Abs Online** 1861-2007/Jul

[File 56] **Computer and Information Systems Abstracts** 1966-2007/Jul

[File 60] **ANTE: Abstracts in New Tech & Engineer** 1966-2007/Jul

[File 65] **Inside Conferences** 1993-2007/Aug 02

[File 99] **Wilson Appl. Sci & Tech Abs** 1983-2007/Jul

NON PATENT LITERATURE/
BIBLIOGRAPHIC FILES

samples in a row of storage devices at time intervals which are determined by a clock signal and is read therefrom after expiration of a **selectable** delay time. Each **storage** device is connectable, via a respective input circuit to a useful signal input and, via a respective output circuit, to a useful signal output. The... ... device being activatable, together with the output circuit of the next storage device in the row, by a respective activation device, which includes a shift **register** device formed by **a** chain of bistable trigger circuits in which the output of each of the trigger circuits is connected to the input of the next trigger circuit in the chain, each activation device including one of the trigger circuits and all trigger circuits being **switched** by the clock **signal**, and also comprising a command device which applies a (first) start pulse to the first trigger circuit in the shift **register** device at a **first** instant and which enables the shift **register** device to propagate **the** start pulse through the chain of trigger circuits in conformity with the clock signal and which interrupts the propagation of the (first) start pulse at a second instant and at the same time applies a next start pulse to the first trigger circuit in the shift **register** device and enables **the** shift **register** device again to **propagate** said next start pulse, the time interval between the first instance (t1) and the second instant (t10) amounting to a **selectable**, integer **multiple** of **periods** of **the** clock signal, the number (n) of storage devices or trigger circuits corresponding at least to said **multiple** (n) of the **periods** of the clock signal. This circuit arrangement can be simply adapted to a **plurality** of different desired **delay** time values, during operation. ...**Claims:**t10) die Weiterleitung des (ersten) Startimpulses (ST) unterbricht und zugleich der ersten Kippschaltung (**20**) in der Schieberegisteranordnung einen nachsten Startimpuls (ST) zuleitet und die Schiebe **registeranordnung** fur die Weiterleitung dieses nachsten Startimpulses (ST) erneut freigibt, wobei die Zeitspanne zwischen dem ersten (t1) und dem zweiten (t10) Zeitpunkt ein wahlbares, ganzzahliges Vielfaches... ... Taktsignals (CL) betragt und die Anzahl (n) der Speicheranordnungen (**11**) bzw. der Kippschaltungen (**20**) mindestens diesem Vielfachen (n) der Perioden des Taktsignals (CL) entspricht. 1... signal samples in a row of storage devices (11) at time intervals determined by a clock signal (CL) and is read therefrom after expiration of **a** selectable delay time, each storage device (11) being connectable, via a respective input circuit (12), to a useful signal input (30) and, via a respective... ... device (11) being activatable, together with the output circuit (13) of the next storage device (11) in the row, by a respective activation device (14, **15**, 20), comprising a **shift** register device formed by a chain of bistable trigger circuits (20) in which the output (25) of each of the trigger circuits (20) is connected... ... next trigger circuit (20) in the chain, each activation device (14, 15,20) comprising one of the trigger circuits (20) and all trigger circuits (20) **being** switched by the clock signal (CL), and also comprising a command device (35) **which** applies a first start pulse (ST) to the first trigger circuit (20) in the **shift** register device at a first instant (t1), enables the **shift** register device to propagate the start pulse (ST) through the chain of trigger circuits (20) in conformity with the clock signal (CL), and interrupts the propagation of the first start **pulse** (ST) at a second instant (t10) and at the same time applies a next start pulse (ST) to the first trigger circuit (20) in the **shift** register device **and** enables the **shift** register device again to propagate said **next** start pulse (ST), the time interval between the first instant (t1) and the second instant (t10) amounting to **a** selectable, **integer** multiple of periods of the clock signal (CL),the number (n) of storage devices (11) or trigger circuits (20) corresponding at least to **said** multiple (n) of the periods of the clock signal (CL). I claim: A device for delaying a functional signal **by a** selectable number of discrete clock pulse periods, said device comprising:input means for receiving said functional signal:a series of storage devices each having a... ... a delayed said functional signal, said output means being switchably coupled to said storage elements, and said delayed functional signal being received by said output **means** parallelly from said storage elements;a **shift** register having a series of stages each stage being coupled to a single one of said storage devices;clock means coupled to the **shift** register for recurrently providing shift pulses to said **shift** register; andload means coupled to the **shift** register for providing **at** selectable recurrence intervals a control signal to said **shift** register which control signal is serially shifted through said series of stages and wherein said control signal, when shifted into a particular stage, controls loading of the storage **elements**, which storage element is within the storage device coupled to the particular stage; with the sample of the functional signal and controls unloading of **a** delayed sample of the functional signal which was **stored** in a storage element of a next storage **device** in said series **of** storage devices.

[File 111] **TGG Natl.Newspaper Index(SM)** 1979-2007/Jul 26

[File 144] **Pascal** 1973-2007/Jul W3

[File 239] **Mathsci** 1940-2007/Sep

[File 256] **TecInfoSource** 82-2007/Aug

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23/5,K/8 (Item 8 from file: 2) **Links**
Fulltext available through: ScienceDirect
INSPEC

06399485 **INSPEC Abstract Number:** B9611-1265B-106, C9611-5210B-044
Title: Retiming for circuits with enable registers
Author Martin, H.-G.
Author Affiliation: Dept. EAS Dresden, FhG IIS Erlangen, Dresden, Germany
Conference Title: Proceedings of the 22nd EUROMICRO Conference. EUROMICRO 96. Beyond 2000: Hardware and Software Design Strategies p. 275-80
Editor(s): Milligan, P.; Kuchcinski, K.
Publisher: IEEE Comput. Soc. Press , Los Alamitos, CA, USA
Publication Date: 1995 **Country of Publication:** USA xvii+667 pp.
ISBN: 0 8186 7487 3 **Material Identity Number:** XX96-02656
U.S. Copyright Clearance Center Code: 1089-6503/96/$5.00
Conference Title: Proceedings of EUROMICRO 96. 22nd Euromicro Conference. Beyond 2000: Hardware and Software Design Strategies
Conference Date: 2-5 Sept. 1996 **Conference Location:** Prague, Czech Republic

Language: English **Document Type:** Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper presents a new method for improving the timing behaviour of digital circuits, which contain enable-**registers** and, e.g., come from the high level synthesis. Known techniques optimize all long combinational paths assuming only **one clock cycle** between **registers**. But enable-**registers** cause also paths having more time than **one clock cycle**. The consideration of this paths leads to a larger optimization potential. As a second topic in the presented method a **register** relocation is performed for a circuit containing enable **registers** and D- **Flipflops**. A suitable retiming algorithm is developed for such circuits. (14 Refs)
Subfile: B C
Descriptors: circuit optimisation; high level synthesis; logic CAD; sequential circuits; timing
Identifiers: enable **registers**; circuit retiming; digital circuits; high level synthesis; combinational paths; D-**Flipflops**; retiming algorithm; sequential elements
Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); B0260 (Optimisation techniques); C5210B (Computer-aided logic design); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits)

Title: Retiming for circuits with enable registers
Abstract: This paper presents a new method for improving the timing behaviour of digital circuits, which contain enable-registers and, e.g., come from the high level synthesis. Known techniques optimize all long combinational paths assuming only one clock cycle between registers. But enable-registers cause also paths having more time than one clock cycle. The consideration of this paths leads to a larger optimization potential. As a second topic in the presented method a register relocation is performed for a circuit containing enable registers and D- Flipflops. A suitable retiming algorithm is developed for such circuits.
Identifiers: enable registers; ... ...D-Flipflops;
1995

23/5,K/16 (Item 16 from file: 2) Links
Fulltext available through: USPTO Full Text Retrieval Options
INSPEC

01564555 **INSPEC Abstract Number:** B73034930, C73022798
Title: A new static shift register with dynamic transfer
Author Wiedmann, S.K.; Berger, H.H.
Author Affiliation: IBM, Boeblingen, West Germany
Journal: Solid-State Electronics vol.16, no.9 p. 1007-10

Publication Date: Sept. 1973 **Country of Publication:** UK
CODEN: SSELA5 **ISSN:** 0038-1101

Language: English **Document Type:** Journal Paper (JP)
Treatment: New Developments (N)
Abstract: A new shift **register** of extremely slow d.c. standby power has been implemented in a simplified bipolar transistor technology using 4 mask steps up to metallization and 2 diffusions only. The bit density is 250 bit/mm/sup 2/ with 5 mu m line dimensions, the standby power 0.1 mu W/bit and the cycle time 150 nsec at 150 mu W/bit. The shift **register** features a new operation principle: In standby, it is truly static, whereas for shifting the memory operates dynamically utilizing the effect that a dynamically unbalanced **flip-flop** switches into a definite state. The dynamic charge unsymmetry originates from the state of the previous cell and is shifted to the next **one** after each **clock cycle**. (12 Refs)
Subfile: B C
Descriptors: bipolar transistors; digital integrated circuits; shift **registers**
Identifiers: static shift **register**; dynamic transfer; bipolar transistor technology
Class Codes: B1260 (Pulse circuits other than digital electronics); B1265 (Digital electronics); B2560J (Bipolar transistors); B2570 (Semiconductor integrated circuits); C5120 (Logic and switching circuits)
Title: A new static shift register with dynamic transfer
Abstract: A new shift register of extremely slow d.c. standby power has been implemented in a simplified bipolar transistor technology using 4 mask steps up to metallization and 2... ...mu m line dimensions, the standby power 0.1 mu W/bit and the cycle time 150 nsec at 150 mu W/bit. The shift register features a new operation principle: In standby, it is truly static, whereas for shifting the memory operates dynamically utilizing the effect that a dynamically unbalanced flip-flop switches into a definite state. The dynamic charge unsymmetry originates from the state of the previous cell and is shifted to the next one after each clock cycle.
Descriptors: ...shift registers
Identifiers: static shift register;
1973

23/5,K/37 (Item 12 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options
Ei Compendex(R)

06942914 **E.I. No:** EIP94091394613
Title: Design for a Josephson micro-pipelined processor

Author: Harada, Yutaka; Hioe, Willy; Takagi, Kazumasa; Kawabe, Ushio
Source: IEEE Transactions on Applied Superconductivity v 4 n 2 Jun 1994. p 97-106
Publication Year: 1994
CODEN: ITASE9 **ISSN:** 1051-8223
Language: English
Document Type: JA; (Journal Article) **Treatment:** A; (Applications); X; (Experimental)
Journal Announcement: 9411W1
Abstract: A novel processor with micro-pipelined architecture is proposed for **latch**-type Josephson logic devices. The processor is segmented into **several** operating stages activated by a **multi**-phase power system. Independent **register** groups are allocated to each stage in order to support pipeline processing of **several** instruction streams. This architecture allows building of a fine pipeline pitch processor which is capable of MIMD processing. A 12-bit micro-pipelined Josephson processor, containing an ALU, a multiplier and 16 **registers**, is described. Driven by a 3-phase ac power system, it is able to process 4 instruction streams simultaneously. A pipeline pitch of 3.3 GHz is expected using conventional Josephson device technology. A 4-bit processor design for 12-bit data length is also discussed. (Author abstract) 10 Refs.
Descriptors: *Microcomputers; Josephson junction devices; Computer architecture; Shift **registers**; Pipeline processing systems; Storage allocation (computer); Digital arithmetic; **Electric** power supplies to apparatus ; Logic circuits; Logic gates
Identifiers: Josephson micro-pipelined processor; Josephson logic devices; Multiphase power system; Fine pipeline pitch processor; High **switching** speed; Low power dissipation; Micro pipeline architecture; **Latch** delay
Classification Codes:
722.4 (Digital Computers & Systems); 714.2 (Semiconductor Devices & Integrated Circuits); 722.1 (Data Storage, Equipment & Techniques); 704.2 (Electric Equipment); 721.2 (Logic Elements); 721.3 (Computer Circuits)
722 (Computer Hardware); 714 (Electronic Components); 704 (Electric Components & Equipment); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 70 (ELECTRICAL ENGINEERING)
Abstract: A novel processor with micro-pipelined architecture is proposed for **latch**-type Josephson logic devices. The processor is segmented into **several** operating stages activated by a **multi**-phase power system. Independent **register** groups are allocated to each stage in order to support pipeline processing of **several** instruction streams. This architecture allows building of a fine pipeline pitch processor which is capable of MIMD processing. A 12-bit micro-pipelined Josephson processor, containing an ALU, a multiplier and 16 **registers**, is described. Driven by a 3-phase ac power system, it is able to process 4 instruction streams simultaneously. A pipeline pitch of 3.3...
Descriptors: *Microcomputers; Josephson junction devices; Computer architecture; Shift **registers**; Pipeline processing systems; Storage allocation (computer); Digital arithmetic; **Electric** power supplies to apparatus ; Logic circuits; Logic gates
Identifiers: Josephson micro-pipelined processor; Josephson logic devices; Multiphase power system; Fine pipeline pitch processor; High **switching** speed; Low power dissipation; Micro pipeline architecture; **Latch** delay

23/5,K/40 (Item 15 from file: 8) Links
Fulltext available through: USPTO Full Text Retrieval Options

04839786 **E.I. Monthly No:** EI8512114383 **E.I. Yearly No:** EI85023499
Title: SHIFT REGISTER USING SINGLE LATCH PER STAGE.

Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 6 Nov 1985 p 2656-2657
Publication Year: 1985
CODEN: IBMTAA **ISSN:** 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) **Treatment:** A; (Applications)
Journal Announcement: 8512
Abstract: A shift **register** using only a single **latch** per stage can be designed for reliable shifting by distributing the shift control through a path parallel to the data-scan path, but in the opposite direction. The single-**latch**-per-stage design can be realized also in bidirectionally shiftable **registers** by arranging to have the control-distribution line running parallel to the scan-path and feeding the shift control via a **switch** to **alternate** ends of the line counter to the **selected** scan direction.
Descriptors: *COMPUTERS, DIGITAL--*Shift **Registers**
Identifiers: SINGLE **LATCH** PER STAGE; RELIABLE SHIFTING
Classification Codes:
722 (Computer Hardware); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)
Title: SHIFT REGISTER USING SINGLE LATCH PER STAGE.
Abstract: A shift register using only a single latch per stage can be designed for reliable shifting by distributing the shift control through a path parallel to the data-scan path, but in the opposite direction. The single-latch-per-stage design can be realized also in bidirectionally shiftable registers by arranging to have the control-distribution line running parallel to the scan-path and feeding the shift control via a switch to alternate ends of the line counter to the selected scan direction.
Descriptors: ...Shift Registers
Identifiers: SINGLE LATCH PER STAGE; RELIABLE SHIFTING

23/5,K/41 (Item 16 from file: 8) **Links**
Fulltext available through: USPTO Full Text Retrieval Options

04839770 **E.I. Monthly No:** EI8512114416 **E.I. Yearly No:** EI85023678
Title: REDUCTION OF THE AREA OF A MICROPROCESSOR CHIP USING THE LSSD CHAIN IN SYSTEM MODE.

Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 6 Nov 1985 p 2625-2626
Publication Year: 1985
CODEN: IBMTAA **ISSN:** 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) **Treatment:** A; (Applications)
Journal Announcement: 8512
Abstract: In a microprocessor performing dividing operations with a one-bit non-restoring algorithm, a shift left is performed on the quotient **register** made of LSSD (Level Scan Sensitive Device) **latches**, using the **latch** chain normally devoted to the LSSD test. Using a one-bit non-restoring algorithm, one quotient bit is calculated starting from the high-order to the low-order bit of the two input numbers. Thus at each cycle, the quotient bit has to be **latched** in the quotient **register** and the previous quotient bit has to be shifted into the next left position of the quotient **register**. At the end of the first cycle the most significant bit of the quotient is **latched** in the last position of the quotient **register**, and at the end of the second **cycle**, this bit is left shifted **one** position and the second quotient bit is **latched** in the last position of the **register**, and so on.
Descriptors: *COMPUTERS, MICROPROCESSOR--*Dividing Circuits; LOGIC CIRCUITS
Identifiers: MICROPROCESSOR CHIP; LSSD (LEVEL SCAN SENSITIVE DEVICE) **LATCHES**; QUOTIENT **REGISTER**; **LATCH** CHAIN
Classification Codes:
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)
Abstract: In a microprocessor performing dividing operations with a one-bit non-restoring algorithm, a shift left is performed on the quotient **register** made of LSSD (Level Scan Sensitive Device) **latches**, using the **latch** chain normally devoted to the LSSD test. Using a one-bit non-restoring algorithm, one quotient bit is calculated starting from the high-order to the low-order bit of the two input numbers. Thus at each cycle, the quotient bit has to be **latched** in the quotient **register** and the previous quotient bit has to be shifted into the next left position of the quotient **register**. At the end of the first cycle the most significant bit of the quotient is **latched** in the last position of the quotient **register**, and at the end of the second **cycle**, this bit is left shifted **one** position and the second quotient bit is **latched** in the last position of the **register**, and so on.
Identifiers: MICROPROCESSOR CHIP; LSSD (LEVEL SCAN SENSITIVE DEVICE) **LATCHES**; QUOTIENT **REGISTER**; **LATCH** CHAIN